3-Phase Gate Driver IC

ECN30300S/ECN30301S Product Specification Rev.1

ECN30300S/30301S is a gate driver IC to drive three phase bridges of MOS/IGBT.
This product is based on the conventional products ECN3030/3031F, adopts Hall element inputs (Amp integrated) and HITACHI original wide-angle (Electronic) commutation control method.
They realize low cost system and torque ripple reduction of Brushless DC (BLDC) motor.

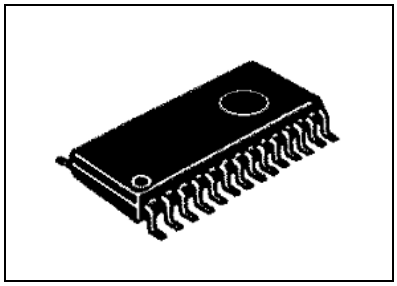
Description

- Integrated 3-Phase BLDC Motor Bridge Driver IC operating from 10 to 185VDC
- Applicable to BLDC motor up to 200W class
- Integrated Charge Pump - Constant TOP Arm bias independent of motor speed
- Integrated 3-Phase Brushless (Electronic) commutation with external Hall sensors
- Integrated wide-angle (Electronic) commutation control method (for torque ripple reduction)
- Integrated Amplifiers for Hall element inputs
- All TOP and BOTTOM Arm gate drive outputs are Push/Pull
- All TOP and BOTTOM Arms switch at up to 20kHz with an on-chip OSC/PWM
- Latch-Up free monolithic IC using a high voltage Dielectric Isolation (DI) process

Functions

- Simple Variable Speed Control via a single (VSP) analog input
- PWM Speed Control without requiring a Microcontroller
- Tachometer - Generates a speed signal (FG)
  ECN30300S - (RPM/60) x (P/2) x3 Hertz
  ECN30301S - (RPM/60) x (P/2) x1 Hertz
- On-Chip 7.5VDC regulator (CB) with a guaranteed External Min load (45mA)
- Over-Current protection is set by an external Sense Resistor (RS)
- Under-Voltage protection for TOP and BOTTOM Arms
- All output IGBT Shut-OFF function

Packaging



Package Type: SOP-28

Block Diagram

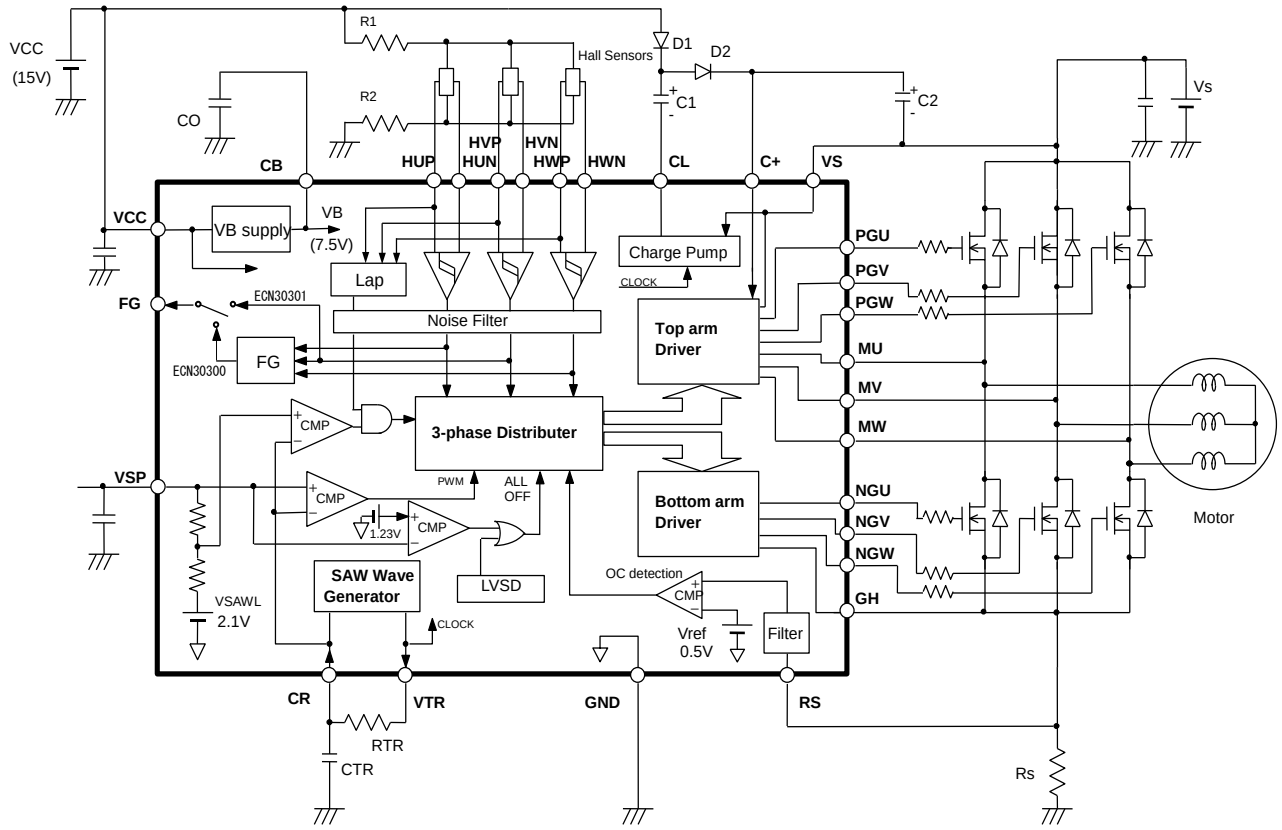


Figure 1 Block Diagram

1. General

(1) Type ECN30300S, ECN30301S
(2) Application 3-Phase BLDC Motor
(3) Structure Monolithic IC
(4) Package SOP-28 Pb Free type SnAg

2. Absolute Maximum Ratings (Ta=25°C)

No.	Item	Symbol	Terminal	Rating	Unit	Condition
1	Output Device Breakdown Voltage	VSM	C+, VS, MU, MV, MW	250	V	
2	Analog Supply Voltage	VCC	VCC	20	V	
3	C+~VS Supply Voltage	VCPM	C+, VS	20	V	
4	Input Voltage	VIN	VSP, RS HUP, HUN, HVP, HVN, HWP, HWN	-0.5~VB+0.5	V	
5	GH Terminal Voltage	VGH	GH	-5~VCC	V	Vcc = 18V max at GH = -5V
6	FG Terminal Voltage	VFG	FG	-0.5~VB+0.5	V	
7	VB Supply Current	IBMAX	CB	50	mA	
8	Junction Operating Temperature	Tjop		-20~+125	°C	Note 1
9	Storage Temperature	Tstg		-40~+150	°C	

Note 1: Thermal Resistance
1) Between junction and air: Rja = 104 °C/W (IC only)
2) Between junction and air: Rja = 82 °C/W (Mounted on PCB size 40x40x1.6mm Wiring density 10%)

3. Electrical Characteristics (Ta=25 °C)

Suffix (T; Top arm, B; Bottom arm, *; phase U, V, W)

No.	Item		Symbol	Terminal	MIN	TYP	MAX	Unit	Condition	
1	Supply Voltage		VSop	VS	10	141	185	V		
2			VCCop	VCC	13.5	15	16.5	V		
3	Standby Current		IS	VS	–	0.3	0.5	mA	VSP=0V, VCC=15V, VS=141V	
4			ICC	VCC	–	3.0	6.0	mA		
5	Output Source Current		IO+T	PG*	60	100	200	mA	20V between C+ and PG*, VCC=15V	
6			IO+B	NG*	130	200	300	mA	10V between VCC and NG*, VCC=15V	
7	Output Sink Current		IO-T	PG*	150	250	350	mA	10V between PG* and M*, VCC=15V	
8			IO-B	NG*	130	200	300	mA	10V between NG* and GH, VCC=15V	
9	High Level Output Voltage		VOHT	C+, PG*	–	5.0	6.0	V	Between C+ and PG* Voltage	IO=0A, VCC=15V
10			VOHB	VCC, NG*	–	–	0.2	V	Between VCC and NG* Voltage	
11	Low Level Output Voltage		VOLT	PG*, M*	–	–	0.2	V	Between PG* and M* Voltage	
12			VOLB	NG*, GND	–	–	0.2	V	Between NG* and GH Voltage	
13	Output Resistance at VTR terminal		RVTR	VTR	–	200	400	Ω	IVTR=±1mA, VCC=15V	
14	SAW Wave	High or Low Level	VSAWH	CR	4.9	5.4	6.1	V	VCC=15V Note 1	
15			VSAWL		1.7	2.1	2.5	V		
16		Amplitude	VSAWW		2.8	3.3	3.8	V	VCC=15V Note 2	

No.	Item		Symbol	Terminal	MIN	TYP	MAX	Unit	Condition
17	Reference Voltage		Vref	RS	0.45	0.5	0.55	V	VCC=15V
18	RS Input Current		IILRS		-100	–	–	μA	VCC=15V, RS=0V Pull Up Resistor Note 3
19	OC Shutdown Delay Time		Tref		–	3.0	6.0	μs	VCC=15V
20	Hall Signal Input	Minimum Differential Voltage	VHOS	HUP, HUN, HVP, HVN, HWP,HWN	60	–	–	mVp-p	VCC=15V
21		Current	IH		–	–	2	μA	
22		Common Mode Voltage Range	VHCM		3	–	VB	V	
23		Hysteresis	VHHYS		20	40	60	mV	
24		Voltage L→H	VHLH		2	20	38	mV	
25		Voltage H→L	VHHL		-38	-20	-2	mV	
26	VSP Input	Current	IVSPH	VSP	–	–	100	μA	VSP=5.0V, VCC=15V Note 4
27		Offset Voltage	SPCOMOF		-40	10	60	mV	VCC=15V Refer to CR terminal
28		All Off Operation	Voff		0.85	1.23	1.6	V	VCC=15V
29	VB Supply Output	Voltage	VB	CB	6.8	7.5	8.2	V	VCC=15V, IB=0A
30		Current	IB		–	–	45	mA	VCC=15V
31	FG Output Voltage and Resistance		RFG	FG	–	200	400	Ω	IFG=±1mA,VCC=15V Note 5
32	LVSD	Detect Voltage	LVSDON	VCC, PG*, NG*	11.0	12.0	12.9	V	Note 6
33		Recover Voltage	LVSDOFF		11.1	12.5	13.0	V	
34	Charge Pump Voltage		VCP	C+, VS	13.0	14.5	–	V	VSP=0V,VCC=15V,VS=141V (at Standby) Note 7

Note 1. See Standard Applications in Section 5, page 9 to set the SAW wave frequency.
Note 2. The amplitude of SAW (i.e., VSAWW) is defined by the following equation:
VSAWW = VSAWH – VSAWL
Note 3. Internal pull up resistors are typically 200 kΩ. The equivalent circuit is shown in Figure 2.
Note 4. The equivalent circuit is shown in Figure 3.
Note 5. The equivalent circuit is shown in Figure 4.
Note 6. The LVSD (Low Voltage Shut Down) function detects and shuts-down at lower VCC.
Note 7. The charge pump voltage (VCP) is defined by the voltage between C+ and VS.

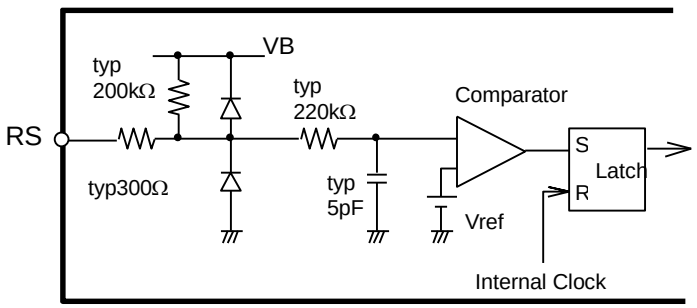


Figure 2. Equivalent circuit around RS terminal

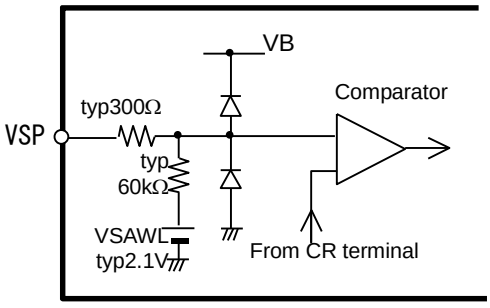


Figure 3. Equivalent circuit around VSP terminal

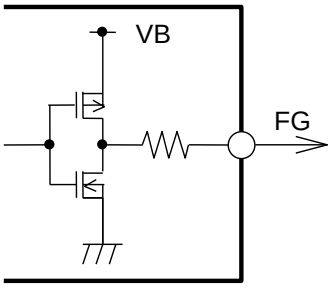


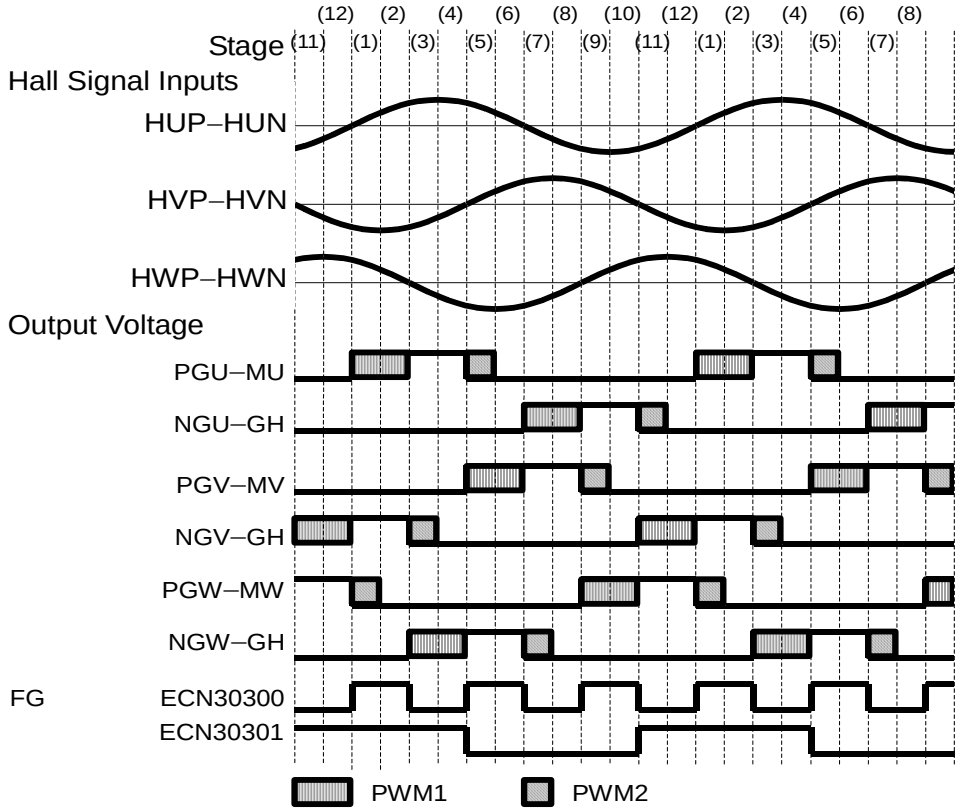
Figure 4. Equivalent circuit around FG terminal

4. Function

4.1 Truth Table

No.	Stage	Inputs						Outputs							
		HUP-HUN	HVP-HVN	HWP-HWN	HUP-HVP	HVP-HWP	HWP-HUP	Phase-U		Phase-V		Phase-W		FG	
								TOP	BOTTOM	TOP	BOTTOM	TOP	BOTTOM	30300	30301
1	1	H	L	H	H	L	H	PWM1	L	L	H	PWM2	L	H	H
2	2	H	L	H	H	L	L	PWM1	L	L	H	L	L	H	H
3	3	H	L	L	H	L	L	H	L	L	PWM2	L	PWM1	L	H
4	4	H	L	L	H	H	L	H	L	L	L	L	PWM1	L	H
5	5	H	H	L	H	H	L	PWM2	L	PWM1	L	L	H	H	L
6	6	H	H	L	L	H	L	L	L	PWM1	L	L	H	H	L
7	7	L	H	L	L	H	L	L	PWM1	H	L	L	PWM2	L	L
8	8	L	H	L	L	H	H	L	PWM1	H	L	L	L	L	L
9	9	L	H	H	L	H	H	L	H	PWM2	L	PWM1	L	H	L
10	10	L	H	H	L	L	H	L	H	L	L	PWM1	L	H	L
11	11	L	L	H	L	L	H	L	PWM2	L	PWM1	H	L	L	H
12	12	L	L	H	H	L	H	L	L	L	PWM1	H	L	L	H

4.2 Timing Chart



Note 1. Inputs H : Input voltage between H**-H** > VHLH
Inputs L : Input voltage between H**-H** < VHHL
Note 2. TOP Arm: Output voltage between PG* and M*
BOTTOM Arm: Output voltage between NG* and GH.
Note 3. PWM1, PWM2 are switching operations by PWM see: item 4.3 PWM Operation.

4.3 PWM Operation

The PWM signal is generated by comparing the input voltage at the VSP pin with the internal SAW wave voltage (available at the CR pin). The Duty Cycle of the resulting PWM signal is thus directly, linearly controlled by the VSP pin voltage: from the Min of VSAWL to the Max of VSAWH.

That is, when VSP is below VSAWL, the PWM duty cycle is at the Minimum value of 0%. When VSP is above VSAWH, the PWM duty cycle is at the Maximum value of 100%.

PWM switching is operated by TOP and BOTTOM arms alternately. This PWM operation is shown as “PWM1” in timing chart (item 4.2).

4.4 Over Current Limit Operation

Over current is detected with the external resistance (Rs). When the RS input voltage exceeds the internal reference voltage (Vref is typically 0.5V), PWM signals (PWM1&PWM2) is fixed at Lo. This Lo state is automatically reset once per internal CLOCK period. If not using this function, connect the RS pin to the GND pin.

4.5 VCC Under-Voltage Detection

If VCC voltage becomes lower than LVSDON (12.0V typ.), all TOP and BOTTOM Arms Shut-OFF.
Normal operation returns when VCC rises above LVSDOFF.

4.6 All TOP and BOTTOM Arm Shut-OFF Function

If VSP terminal voltage becomes lower than Voff(1.23V typ.), all TOP and BOTTOM Arms Shut-OFF.

VSP Input Voltage	TOP and BOTTOM Arm Output
0V ≤ VSP < Voff	All Arms are OFF
Voff ≤ VSP < VSAWL	PWM1&PWM2 periods OFF Following the items 4.1, 4.2
VSP ≥ VSAWL	PWM1&PWM2 periods Active Following the items 4.1, 4.2

When a motor is rotating and all TOP and BOTTOM Arms shut-OFF by a function in items 4.5, 4.6, the VS voltage can rise because of energy regeneration from the motor. In all case, VS must not exceed the 250VDC Breakdown Voltage.

5. Standard Applications

5.1 External Components

Component	Standard Value	Usage	Remark
C0	0.22 μF ± 20%	Filters the internal Power supply (VB)	Stress voltage is VB (=8.2V)
C1, C2	1.0 μF ± 20%	For charge pump	Stress voltage is VCC
D1, D2	Over 250V, 1A trr ≤ 100ns	For charge pump	
Rs	Note 1	Sets Over-Current limit	
CTR	1800 pF ± 5%	Sets PWM frequency	Stress voltage is VB (=8.2V) Note 2
RTR	22 kΩ± 5%		

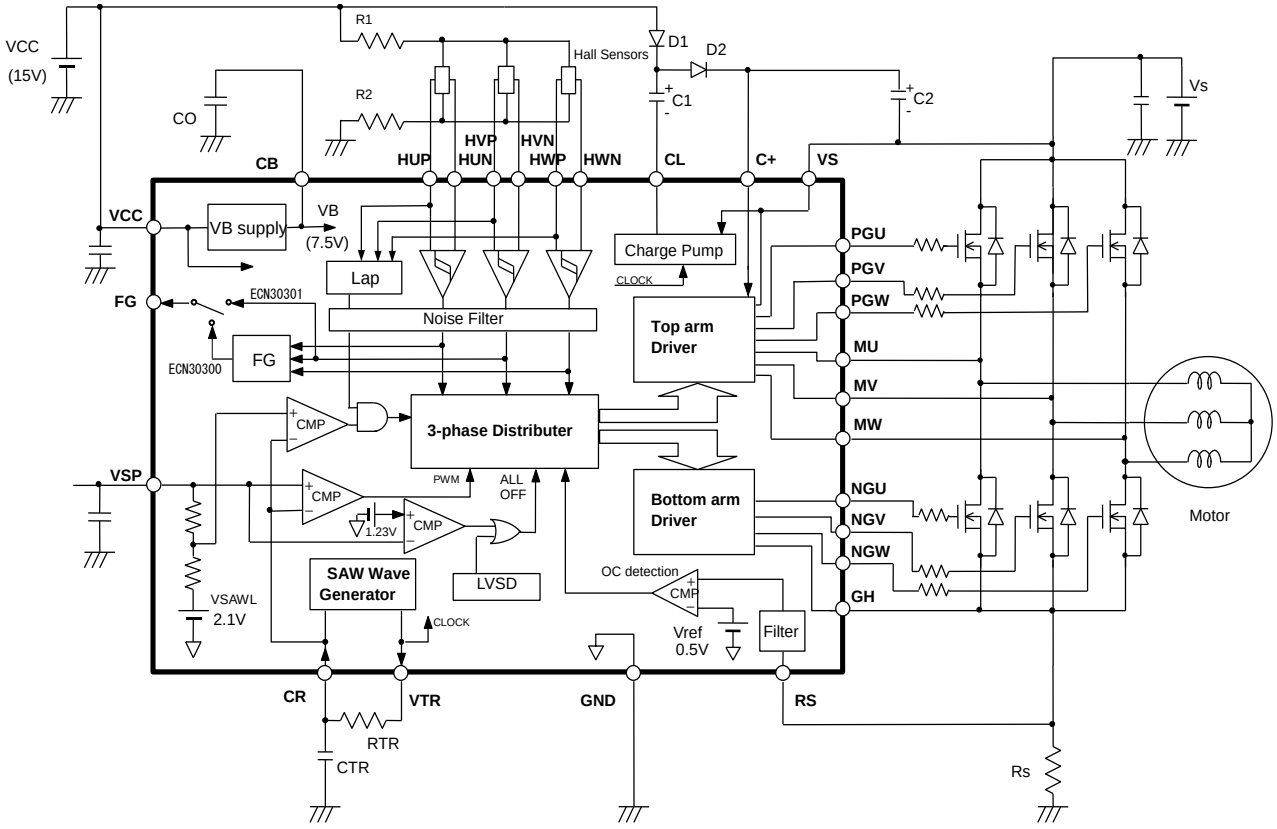
Note 1. The detection current (IO) for the Over Current limit operation can be calculated as follows.

IO(A) = Vref(V) / Rs(Ω)

Where Vref is 0.55V and Rs is a minimum value. (These are worst-case values.)

Note 2. The PWM frequency is approximated by the following equation:

PWM frequency (Hz) ≈ 0.494 / (CTR(F) × RTR(Ω))



Note; The inside of the bold line shows ECN30300/30301

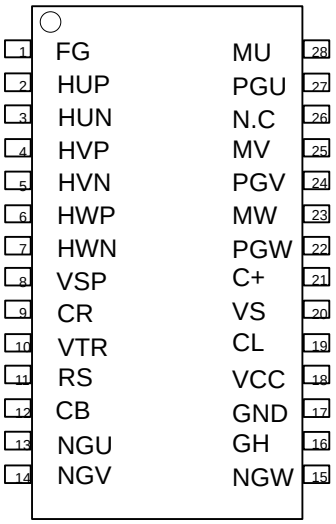
Figure 5. Block Diagram

5.2 Supply Voltage Sequence

The order for turning on power supplies should be (1)Vcc, (2)VS, (3)VSP. The order for turning off should be (1)VSP, (2)VS, (3)Vcc. When the order is different from these orders, the external switching devices (MOSFET, IGBT) can be thermally broken.

This is because the saturation voltage of the switching devices may rapidly increase, when gate voltages decrease.

6. Pinout



(Marking Side)

Figure 6. Pin Connections

7. Terminal definitions

Terminal No.	Symbol	Definition	Remark
1	FG	Tachometer output signal. Frequency is (RPM/60)×(P/2)×3 Hz by ECN30300, and (RPM/60)×(P/2)×1 Hz by ECN30301.	
2	HUP	Plus Input signal from the Hall element of phase-U	
3	HUN	Minus Input signal from the Hall element of phase-U	
4	HVP	Plus Input signal from the Hall element of phase-V	
5	HVN	Minus Input signal from the Hall element of phase-V	
6	HWP	Plus Input signal from the Hall element of phase-W	
7	HWN	Minus Input signal from the Hall element of phase-W	
8	VSP	Input analog voltage that varies the PWM duty cycle from 0% to 100%	
9	CR	Connect resistor & capacitor to generate the PWM clock frequency	
10	VTR	Connect resistor to generate the PWM clock frequency	
11	RS	Rs voltage input for over current limit operation	
12	CB	Internal regulated (VB) power supply output	
13	NGU	BOTTOM Arm Gate Drive for Phase-U	
14	NGV	BOTTOM Arm Gate Drive for Phase-V	
15	NGW	BOTTOM Arm Gate Drive for Phase-W	
16	GH	BOTTOM Arm Reference Terminal. Connect RS.	
17	GND	Analog ground	
18	VCC	Analog/Logic power supply	
19	CL	For the Charge Pump circuit	Note1
20	VS	BLDC Motor Power Bus	Note1
21	C+	For the Charge Pump circuit, power supply for Top Arm drive circuit	Note1
22	PGW	TOP Arm Gate Drive for Phase-W	Note1
23	MW	TOP Arm Reference Terminal for Phase-W	Note1
24	PGV	TOP Arm Gate Drive for Phase-V	Note1
25	MV	TOP Arm Reference Terminal for Phase-V	Note1
26	N.C	No Connection	Note2
27	PGU	TOP Arm Gate Drive for Phase-U	Note1
28	MU	TOP Arm Reference Terminal for Phase-U	Note1

Note1 This is high voltage pin. Recommend coating processing to keep the insulation.
Note2 Not connected to the internal IC chip.

8. Inspection

Hundred percent inspections shall be conducted on electric characteristics at room temperature (25±5°C).

9. Cautions

9.1 Customers are advised to follow the below cautions to protect semiconductor from electrical static discharge (ESD).

a) IC needs to be dealt with caution to protect from damage by ESD. Material of container or any device to carry semiconductor devices should be free from ESD, which may be caused by vibration while transportation. To use electric-conductive container or aluminum sheet is recommended as an effective countermeasure.

b) What touches semiconductor devices such as work platform, machine and measuring and test equipment should be grounded.

c) Workers should be grounded connecting with high impedance around 100kΩ to 1MΩ while dealing with semiconductor to avoid damaging IC by electric static discharge.

d) Friction with other materials such as a high polymer should not be caused.

e) Attention is needed so that electric potential will be kept on the same level by short circuit terminals when PC board with mounted IC is carried and that vibration or friction might not occur.

f) Air conditioning is needed so that humidity should not drop.

9.2 Applying molding or resin coating is recommended for below mentioned pin-to-pin insulation;
19-25, 27-28

9.3 Refer to “Precautions for Use of High-Voltage Monolithic ICs” for the other precautions and instructions on how to deal with products.

9.4 Regardless of changes in external conditions during use, “absolute maximum ratings” should never be exceeded in designing electronic circuits that employ products. In a case absolute maximum ratings are exceeded, products may be damaged or destroyed. In no event shall Hitachi be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.

9.5 Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure.

9.6 Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers.

Hitachi, Ltd. assumes no liability for applications assistance, customer product design, or performance. In such cases, it is advised customers to ensure circuit and/or product safety by using semiconductor devices that assures high reliability or by means of user’s fail-safe precautions or other arrangement. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

9.7 The figure below shows recommended mounting condition by the reflow.
Reflow to ”Precautions for Use of High-Voltage Monolithic ICs” for details.

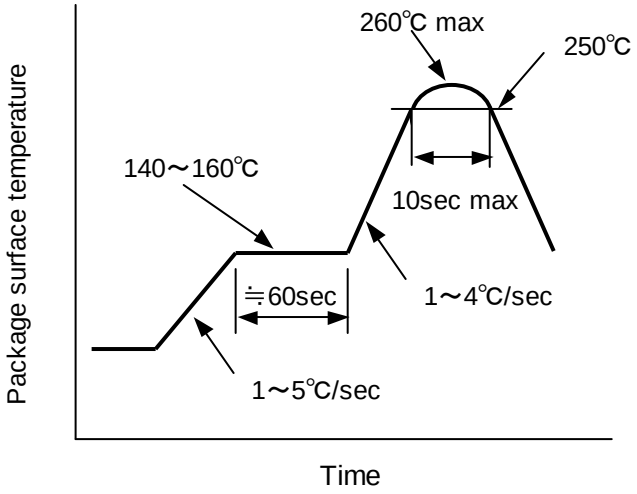


Figure 7. Infrared reflow and air reflow Recommended condition

10. Important Notices

10.1 Hitachi warrants performance of its power semiconductor products (hereinafter called “products”) to the specifications applicable at the time of sale in accordance with the Product Specification. Testing and other quality control techniques are utilized to the extent Hitachi needs to meet specifications described in the Product Specification. Specific testing of all parameters of each device is not necessarily performed, except those mandated by related laws and/or regulations.

10.2 Should any claim be made within one month of product delivery about products’ failure to meet performance described in the Product Specification, all the products in relevant lot(s) shall be re-tested and re-delivered. Products delivered more than one month before of such claim shall not be counted for such response.

10.3 Hitachi assumes no obligation or any way of compensation should any fault about customer’s goods using products be found in marketplace. Only in such a case fault of Hitachi is evident and products concerned do not meet the Product Specification, compensation shall be conducted if claimed within one year of product delivery up to in the way of product replacement or payment of equivalent amount.

10.4 Hitachi reserves the right to make changes in the Product Specification and to discontinue mass production of the relevant products without notice. Customers are advised before purchasing to confirm specification of the product of inquiry is the latest version and that the relevant product is on mass production status in such a case purchasing is suspended for one year or more.

10.5 In no event shall Hitachi be liable for any damage that may result from an accident or any other cause during operation of the user’s units according to this Product Specification. Hitachi assumes no responsibility for any intellectual property claims or any other problems that may result from applications of information, products or circuits described in this Product Specification.

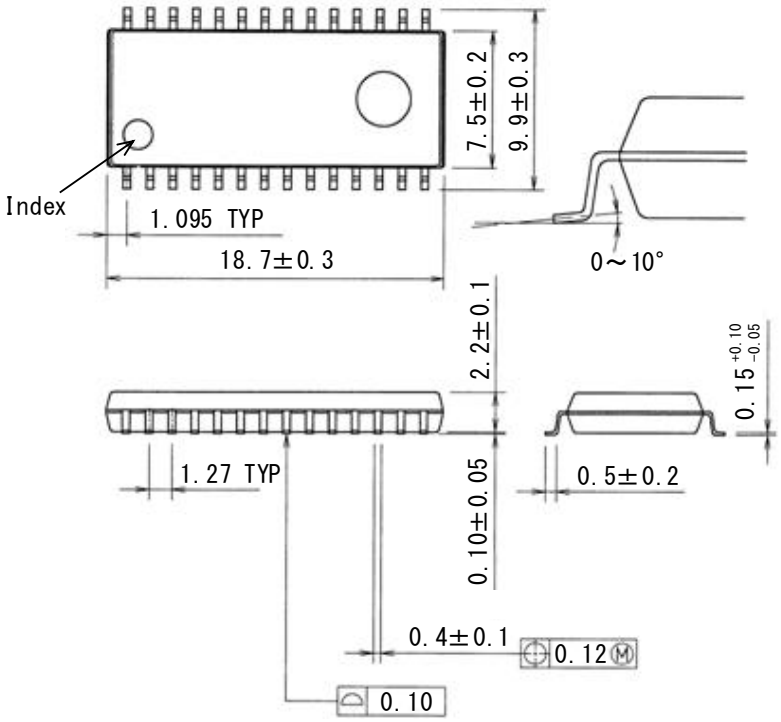
10.6 No license is granted by this Product Specification under any patents or other rights of any third party or Hitachi, Ltd.

10.7 This Product Specification may not be reproduced or duplicated, in any form, in whole or in part without the expressed written permission of Hitachi, Ltd.

10.8 The products (technologies) described in this Product Specification are not to be provided to any party whose purpose in their application will hinder maintenance of international peace and safety nor are they to be applied to that purpose by their direct purchasers or any third party. When exporting these products (technologies), the necessary procedures are to be taken in accordance with related laws and regulations.

11. Appendix

11.1 Package Dimensions (Unit: mm)



11.2 Switching Operation in Phase Commutation (Torque Ripple Reduction Control)

This IC has overlapped energizing period of 30 electrical angle degrees in phase commutation. Figure 8 shows an example of Phase-U motor current waveform when the phase is switched from U to V.

The duty of "PWM2" is about 1/2 against the duty of "PWM1". For instance, the PWM2 duty is 40% when the PWM1 duty is 80%.

Figure 9 shows an example of motor current waveform of ECN3030 and ECN3031. They adopt conventional 120-degree commutation method. In this case, the motor current decreases rapidly because the voltage between MU and MW becomes minus after the phase switch.

On the other hand, the current decreases slowly after the phase switch in Figure 8. Therefore, the motor torque is smoothed, and the torque ripple is decreased.

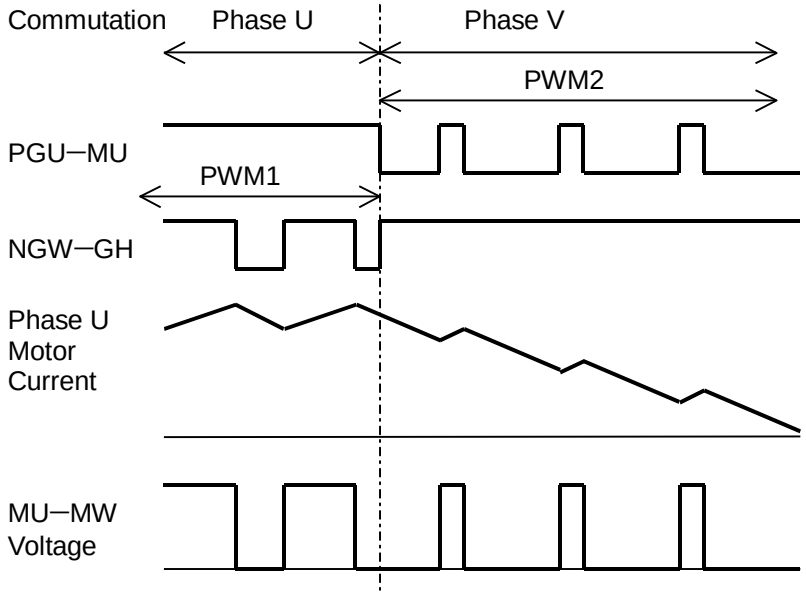


Figure 8 Example for Phase U motor current waveform by ECN30300/30301 Control in phase Commutation from U to V (Stage (4)→(5) in 4.2 Timing chart)

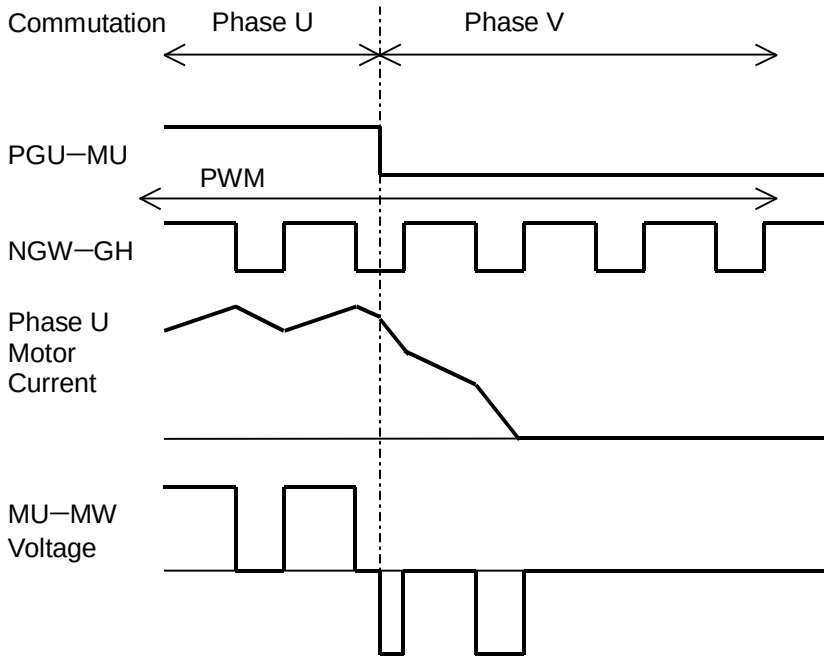


Figure 9 Example for Phase-U motor current waveform by ECN3030/3031 Control in phase Commutation from U to V

11.3 About torque ripple reduction control (wide-angle commutation control)

Overlapped energizing period in phase commutation is set to 30 electrical angle degrees when Hall signal is sine wave. This is achieved by voltage comparison of two signals from Hall signal terminal HUP, HVP, HWP.

When overlapped energizing period is long, there is a tendency that the passive current increases and the efficiency decreases; on the other hand, when overlapped energizing period is short, the drastic change in current cannot be controlled, and torque ripple reduction effect cannot be achieved.

As a way of prevention, it is necessary to pay attention to following.

- Input Hall signals with minimized sine wave distortion
- Minimize variance of the size and phase of three-phase Hall signal
- Prevent noise overlay in Hall signal

For example, magnetize a rotor to generate a sine wave induced voltage, select minimum variation Hall element, and put a noise elimination capacitor for Hall input or similar countermeasures are required.

11.4 About Hall element installation position

Figure 10 shows an example of an installation position of Hall elements for motor induced voltage.

By adjustment of an installation position, the efficiency of a motor and the amplitude of torque ripple can be changed.

Adjust an installation position by testing with the actual system.

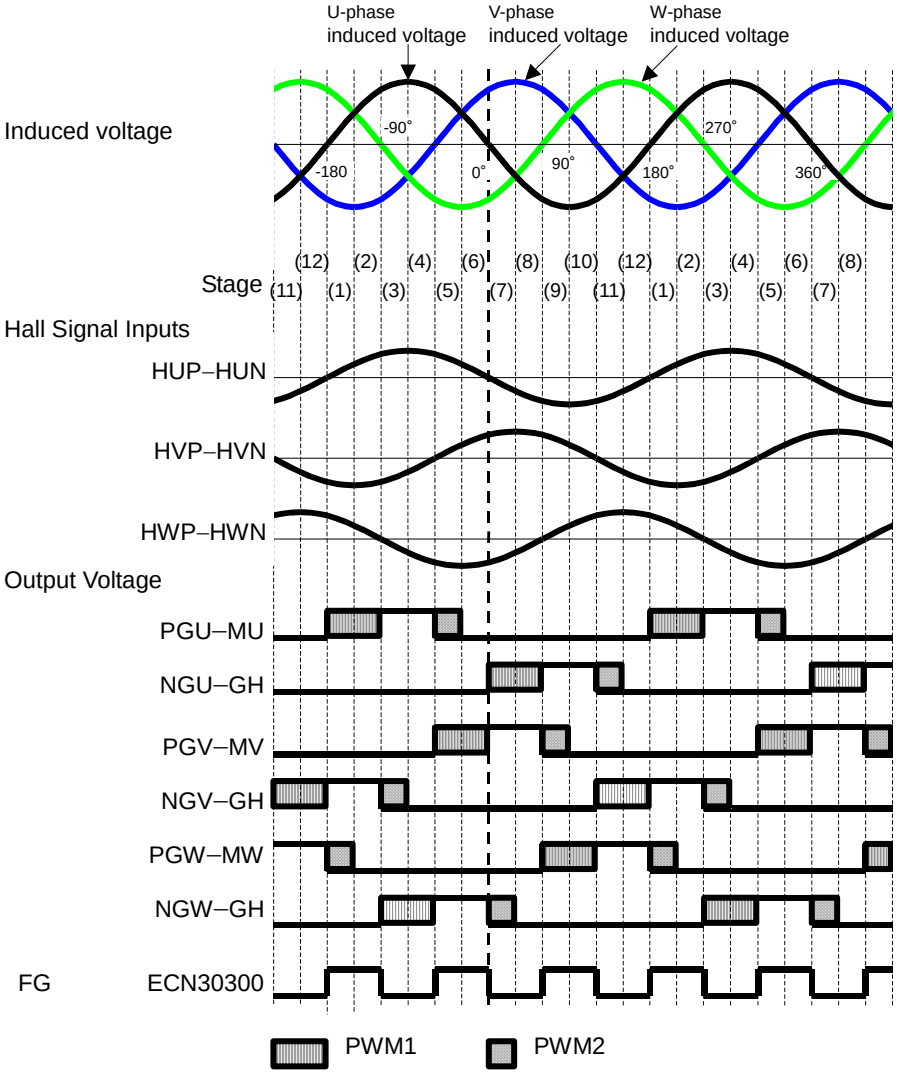


Figure 10 Example of Hall Elements Installation Position (For Forward Rotation)

11.5 About use by reverse rotation

Figure 11 shows timing chart of reverse rotation of a motor. In reverse rotation, there is not an overlap period after phase switch shown in the timing chart of item 4.2. In this case, the motor current decreases rapidly after the phase switch. Therefore, there is not an effect of torque ripple reduction control.

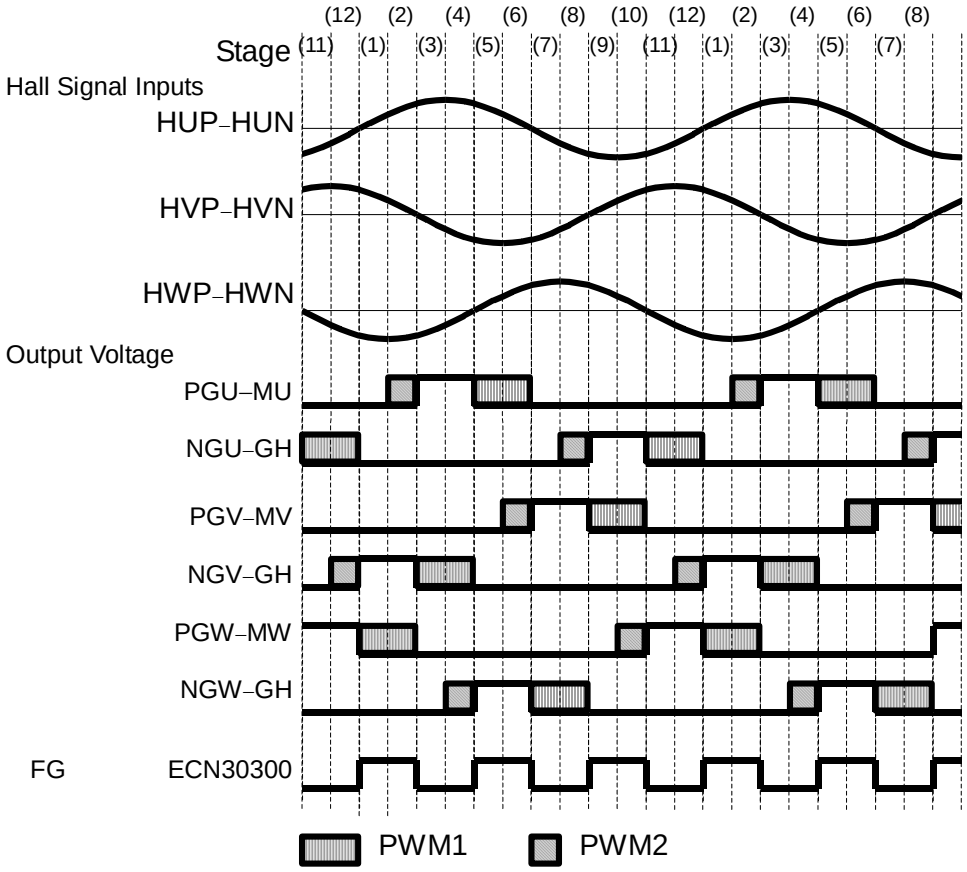


Figure 11 Timing Chart of Reverse Rotation

11.6 The use of Hall IC

It is not recommended to use Hall ICs because of the following problems.

- Overlapped energizing periods become 60 electrical angle degrees (See Figure 12) and unstable.
- Reactive current is increased and motor efficiency can be decreased.

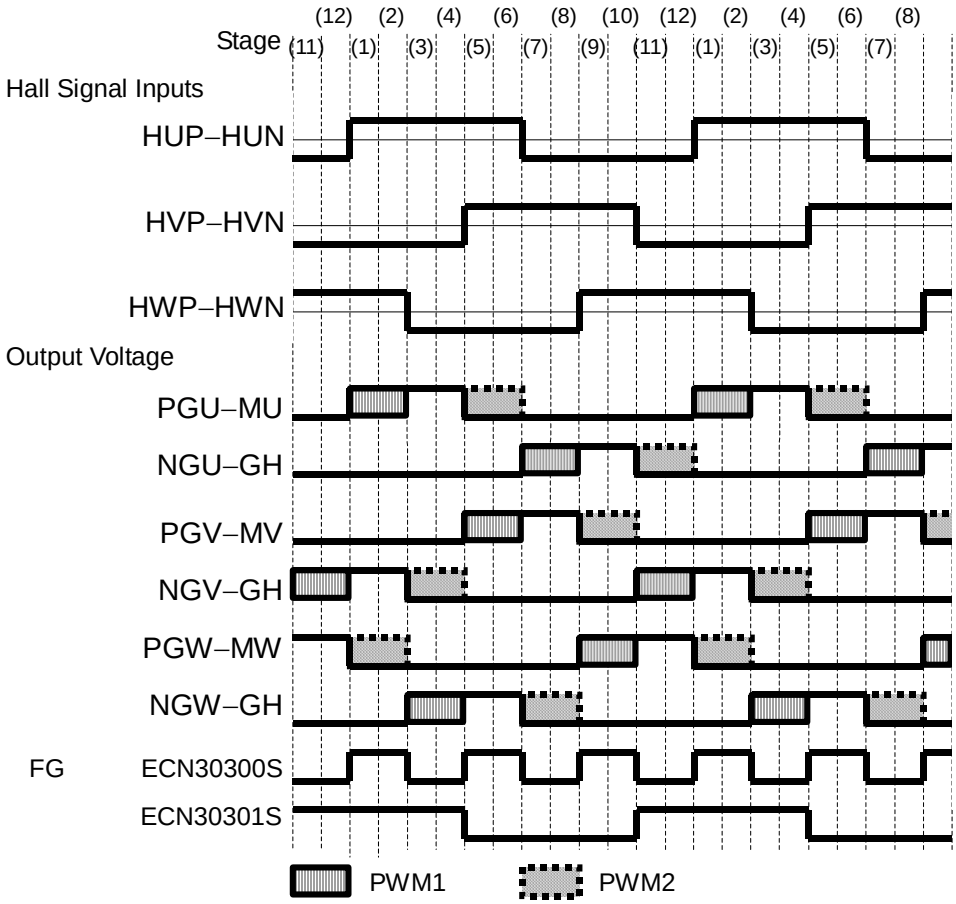


Figure 12 Hall IC using the example of timing chart

Precautions for Safe Use and Notices

If semiconductor devices are handled inappropriate manner, failures may result. For this reason, be sure to read the latest version of "Instructions for Use of Hitachi High-Voltage Monolithic ICs" before use.

⚠ This mark indicates an item about which caution is required.

⚠ **CAUTION** This mark indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury and damage to property.

⚠ CAUTION

(1) Regardless of changes in external conditions during use "absolute maximum ratings" should never be exceed in designing electronic circuits that employ semiconductors. In the case of pulse use, furthermore,"safe operating area (SOA)"precautions should be observed.

(2) Semiconductor devices may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure.

(3) In cases where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment), safety should be ensured by using semiconductor devices that feature assured safety or by means of user's fail-safe precautions or other arrangement. Or consult Hitachi's sales department staff.

(If a semiconductor devices fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst)

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