3-Phase Motor Driver IC
ECN30622S Product Specification Rev. 1

1. Product Description

1.1 Features

(1) Maximum Ratings: 600VDC/3.0A, suitable for the system from 200VAC to 240VAC
(2) PWM control of top and bottom arm IGBTs is possible with six control signals
(3) Six IGBTs, six FWDs (Free-Wheeling Diodes), drivers for IGBTs, protection circuits, etc. integrated into a single chip, resulting in space reduction
(4) Drives a motor using a high voltage DC power supply and a low voltage DC power supply (15V)
(5) Motor under free run condition detected by built-in back EMF detection circuit

1.2 Functions

(1) Back EMF detection (Three-phase)
(2) Prevention function against simultaneous ON of top and bottom arm IGBTs
(3) Charge pump circuit (Built-in clock circuit and high voltage diodes)
(4) Current limit (detects at 0.5V)
(5) Over-current protection (detects at 1.0V, selectable reset method)
(6) Over temperature protection
(7) Fault function
(8) Vcc low-voltage detection
(9) 5V power supply circuit, 7.5V power supply circuit

1.3 Block Diagram

FIGURE 1.3.1 shows block diagram.

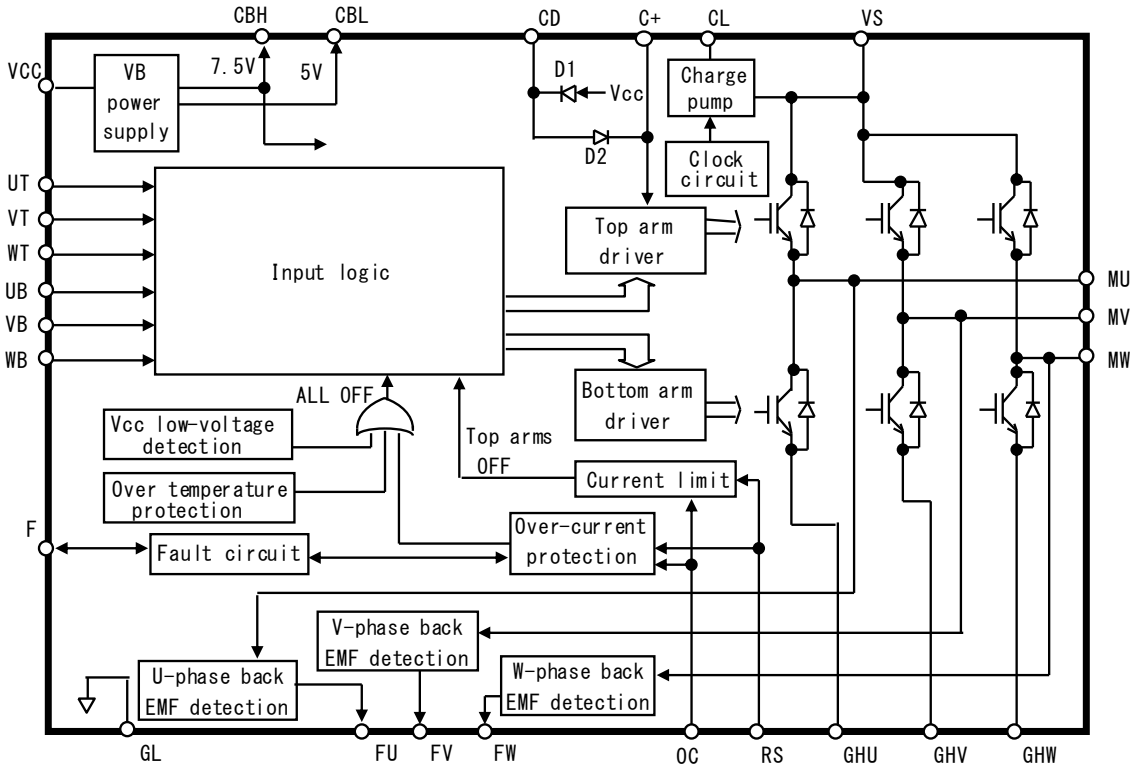
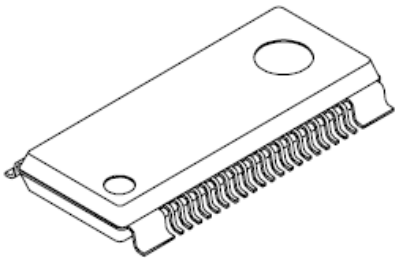


FIGURE 1.3.1 Block Diagram

1.4 Package



(Package: HSOP-37N)

FIGURE 1.4.1 Package of ECN30622S

2. Specification

2.1 Maximum Ratings

TABLE 2.1.1 Maximum Ratings Condition: Ta=25℃

No.	Item		Symbol	Pin	Rating	Unit	Condition
1	Output device withstand voltage		VSM	VS, CL, CD MU, MV, MW	600	V	
2	Vcc power supply voltage		VCC	VCC	18	V	
3	Voltage between C+ and VS		VCPM	C+, VS	18	V	
4	Input voltage 1		VIN1	UT, VT, WT, UB, VB, WB, RS	−0.5 to VBH+0.5	V	
5	Input voltage 2		VIN2	OC	−0.5 to Vcc+0.5	V	
6	Output current	Pulse	IP	MU, MV, MW	3.0	A	Note 1
7		DC	IDC		2.0		
8	Fault output voltage		Vflt	F	−0.5 to Vcc+0.5	V	
9	FU, FV, FW output voltage		VFU, VFV, VFW	FU, FV, FW	−0.5 to VBH+0.5	V	
10	VB supply output current		IBMAX	CBL, CBH	50	mA	Note 2
11	Junction operating temperature		Tjop	—	−40 to +135	℃	Note 3
12	Storage temperature		Tstg	—	−40 to +150	℃	

Note 1: Output IGBTs can handle this peak current.
Note 2: Total value of CBL and CBH.
Note 3: Thermal resistance
Between junction and case: Rjc = 3℃/W (Reference value)

2.2 Electrical Characteristics

TABLE 2.2.1 Electrical Characteristics Suffix (T: Top arm, B: Bottom arm) Condition: Ta=25℃

No.	Item		Symbol	Pin	Min.	Typ.	Max.	Unit	Condition
1	Standby current		ISH	VS	—	0.1	0.4	mA	UT,VT,WT,UB,VB,WB=0V
2			ICC	VCC	—	5	10	mA	VS=325V, VCC=15V, IBL, IBH=0A
3	IGBT collector-emitter saturation voltage		VONT	MU, MV, MW	—	2.0	3.0	V	I=0.7A, VCC=15V
4			VONB		—	2.0	3.0	V	
5	Free-wheeling diode forward voltage		VFDT	MU, MV, MW	—	1.6	2.8	V	I=0.7A
6			VFDB		—	1.6	2.8	V	
7	Output delay time	Turn ON	TdONT	MU, MV, MW	—	0.7	1.1	μs	VS=325V, VCC=15V I=0.7A, Resistance load
8			TdONB		—	0.7	1.1	μs	
9		Turn OFF	TdOFFT		—	0.7	1.1	μs	
10			TdOFFB		—	0.7	1.1	μs	
11	Minimum pulse width		TMINB	MU, MV, MW	0.5	—	—	μs	VCC=15V Note 1
12	Current limit	Reference voltage	Vref1	RS	0.45	0.50	0.55	V	VCC=15V
13		Delay time	Tref1		—	2.0	4.5	μs	
14	Over-current protection	Reference voltage	Vref2	RS, F	0.9	1.0	1.1	V	VCC=15V
15		Delay time	Tref2		—	1.7	3.0	μs	
16		Recovery time	Trs		—	1.0	2.0	ms	VCC=15V, CF=1000pF, RF=820kΩ, OC=VCC, Connect RF to CBL.
17	RS input current		IILRS	RS	−100	—	—	μA	VCC=15V, RS=0V Note 2
18	Over temperature protection	Operating temperature	TSDON	MU, MV, MW	135	160	185	℃	VCC=15V
19		Hysteresis	TSDHYS		—	25	—	℃	
20	Vcc low-voltage detection	Operating voltage	LVSDON	VCC, MU, MV, MW	11.0	12.0	12.9	V	
21		Recovery voltage	LVSDOFF		11.1	12.5	13.0	V	
22	UT,VT,WT, UB,VB,WB inputs	Voltage	VIH	UT, VT, WT, UB, VB, WB	3.0	—	—	V	VCC=15V
23			VIL		—	—	1.0	V	
24		Current	IIH		—	—	100	μA	Input=5V VCC=15V Pull-down resistor Note 3
25			IIL		−10	—	—	μA	Input =0V VCC=15V
26	VBL supply output	Voltage	VBL	CBL	4.5	5.0	5.5	V	VCC=15V, IBL=0A
27		Current	IBL		—	—	45	mA	VCC=15V Note 4
28	VBH supply output	Voltage	VBH	CBH	6.8	7.5	8.2	V	VCC=15V, IBH=0A
29		Current	IBH		—	—	45	mA	VCC=15V Note 4
30	Fault reset input time		Tflrs	F	—	15	30	μs	VCC=15V, OC=GL or CBH
31	F output resistance		RONF	F	—	0.9	1.8	kΩ	Note 5
32	FU, FV, FW output resistance		RONFU, RONFV, RONFW	FU, FV, FW	—	0.8	1.6	kΩ	Note 6
33	Charge pump diode forward voltage		VFDCP	VCC, CD, C+	—	0.8	1.4	V	I=1mA
34	Back EMF detection level		VIHE	MU, MV, MW	4	—	—	V	VCC=15V, UT,VT,WT,UB,VB,WB=0V
35			VILE		—	—	1	V	

Note 1: The minimum pulse width to be able to turn on and off top and bottom arms.
Note 2: Internal pull-up resistor is typically 200kΩ. The equivalent circuit is shown in FIGURE 2.2.1.
Note 3: Internal pull-down resistor is typically 200kΩ. The equivalent circuit is shown in FIGURE 2.2.2.
Note 4: The total value of IBL and IBH must be the IBMAX maximum rating or lower.
Note 5: The equivalent circuit is shown in FIGURE 2.2.3.
Note 6: The equivalent circuit is shown in FIGURE 2.2.4.

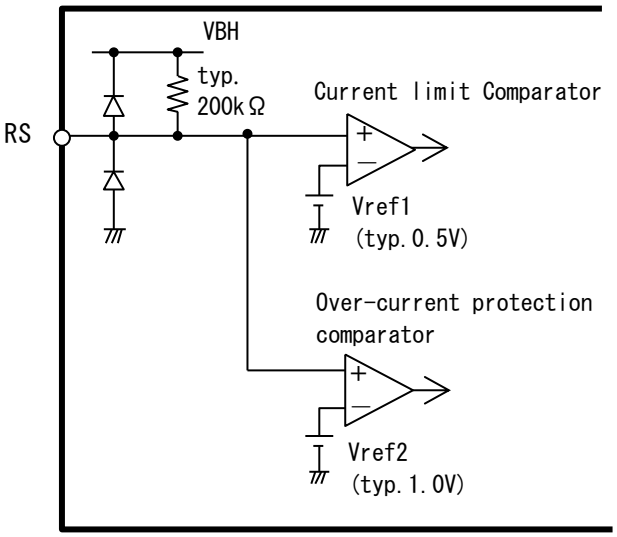


FIGURE 2.2.1 Equivalent Circuit around RS Pin

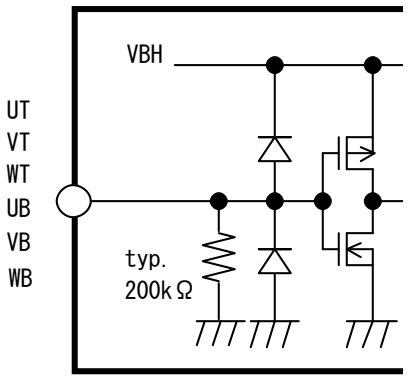


FIGURE 2.2.2 Equivalent Circuit around UT, VT, WT, UB, VB, WB Pins

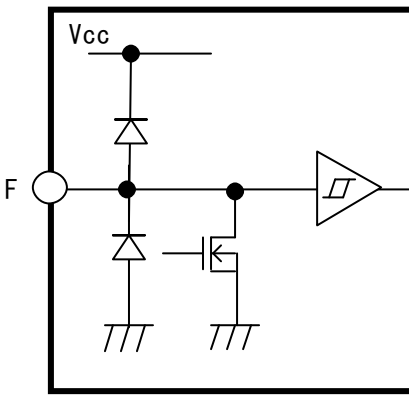


FIGURE 2.2.3 Equivalent Circuit around F Pin

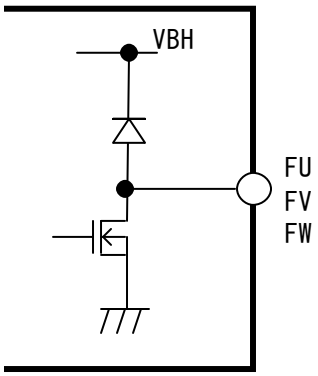


FIGURE 2.2.4 Equivalent Circuit around FU, FV, FW Pins

2.3 Operating Condition

TABLE 2.3.1 Operating Condition

No.	Item	Symbol	Pin	Min.	Typ.	Max.	Unit	Condition
1	Supply voltage	VSop	VS	50	325	450	V	
2		VCCop	VCC	13.5	15.0	16.5	V	
3	GH voltage	Vgh	GHU, GHV, GHW	−1.2	—	1.2	V	Based on GL pin

2.4 Functions and Operations

2.4.1 Truth Table

TABLE 2.4.1.1 Truth Table

Input UT, VT, WT UB, VB, WB	IGBT operation
L	OFF
H Note 1	ON

Note 1: When the top input and bottom input in the same phase are “H” simultaneously, the top and bottom arm IGBTs in this phase are both off.

2.4.2 Current Limit

When the voltage at the RS pin exceeds the current limit reference voltage (Vref1, typ. 0.5V), the top arm IGBTs are all turned off. When each of the input UT, VT, and WT is “L”, this limit operation is individually reset in each phase. “L” is not outputted to the F pin in this function operation.

2.4.3 Over-current Protection

When the voltage at the RS pin exceeds the over-current protection reference voltage (Vref2, typ. 1.0V), the F output is “L”, and the top and bottom arm IGBTs are all turned off. When this function is not used, connect the F pin to the VCC pin. Section 2.4.4 describes how to reset this protection operation.

2.4.4 OC Setting Method

The settings of the OC pin depend on whether to use the current limit or not and how to reset the over-current protection operation. Connect the OC pin to the GL pin, CBH pin, or VCC pin based on your preference (see TABLE 2.4.4.1). FIGUREs 2.4.4.1, 2.4.4.2, and 2.4.4.3 show the timing charts of the protection functions in each setting.

TABLE 2.4.4.1 OC Setting Method

Connected pin	Current Limit	Method for resetting over-current protection operation	Timing chart
GL	Enable	Holding All inputs “L” (Reset after holding “L” for more than the Fault reset input time (Tflrs))	FIG. 2.4.4.1
CBH	Disable		FIG. 2.4.4.2
VCC	Disable	Automatically (Reset after the recovery time (Trs) passes)	FIG. 2.4.4.3

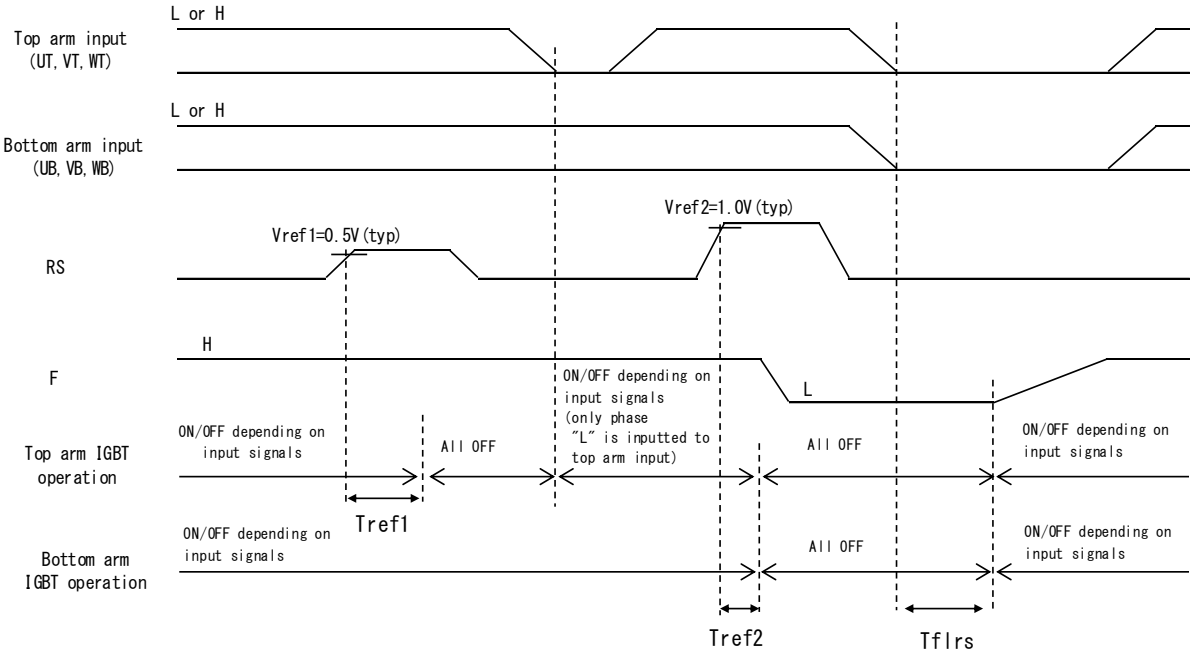


FIGURE 2.4.4.1 Timing Chart in Case of OC Connected to GL

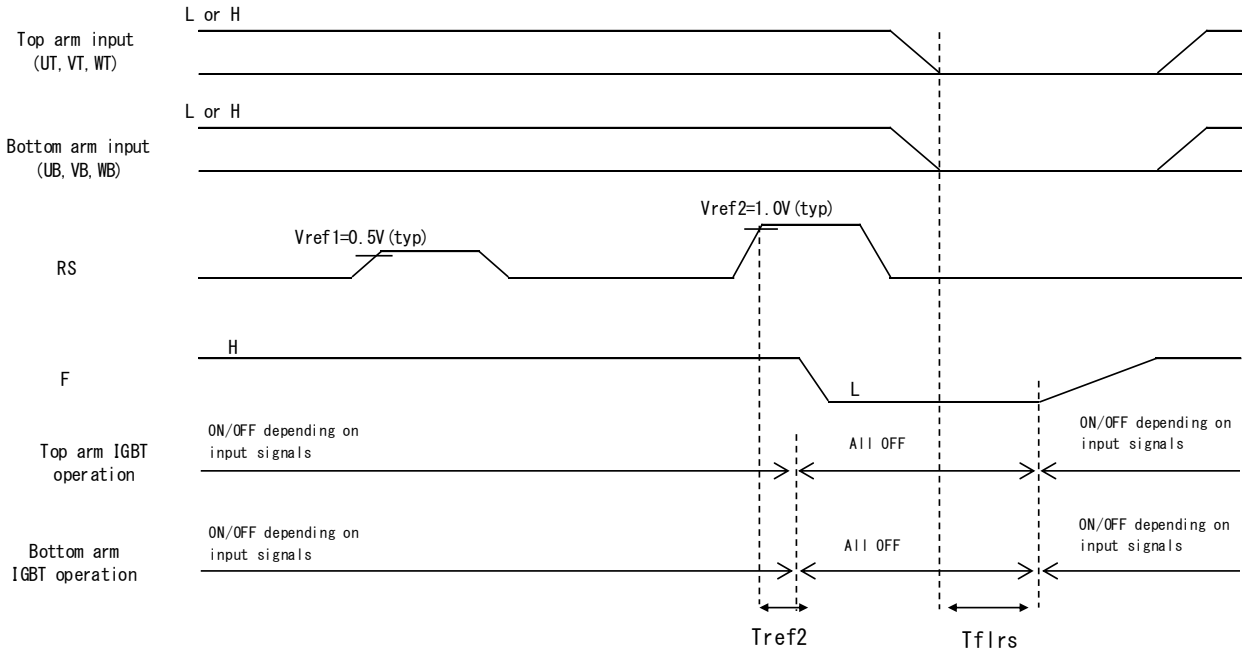


FIGURE 2.4.4.2 Timing Chart in Case of OC Connected to CBH

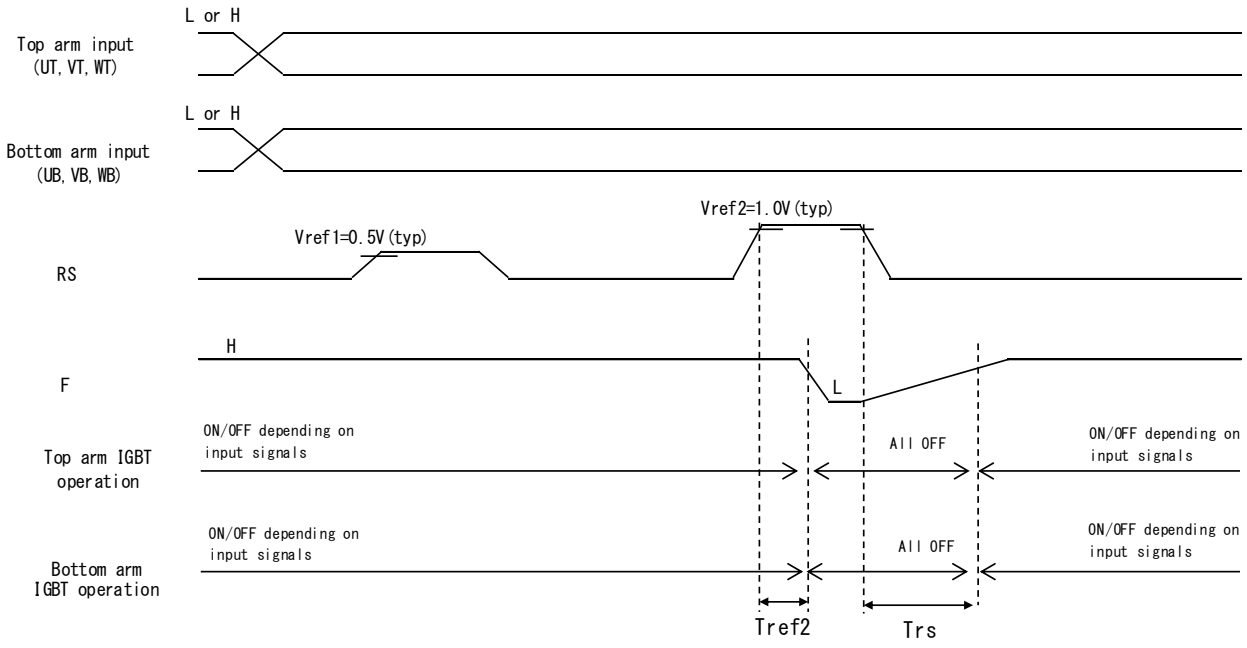


FIGURE 2.4.4.3 Timing Chart in Case of OC Connected to VCC

2.4.5 Vcc Low-voltage Detection

When the Vcc voltage drops below the operating voltage of the Vcc low-voltage detection (LVSDON), all IGBTs (top and bottom arms) are turned off. When the Vcc voltage goes up above the recovery voltage of the Vcc low-voltage detection (LVSDOFF), the IC returns to the state in which the IGBTs operate depending on input signals. “L” is not outputted to the F pin in this function operation.

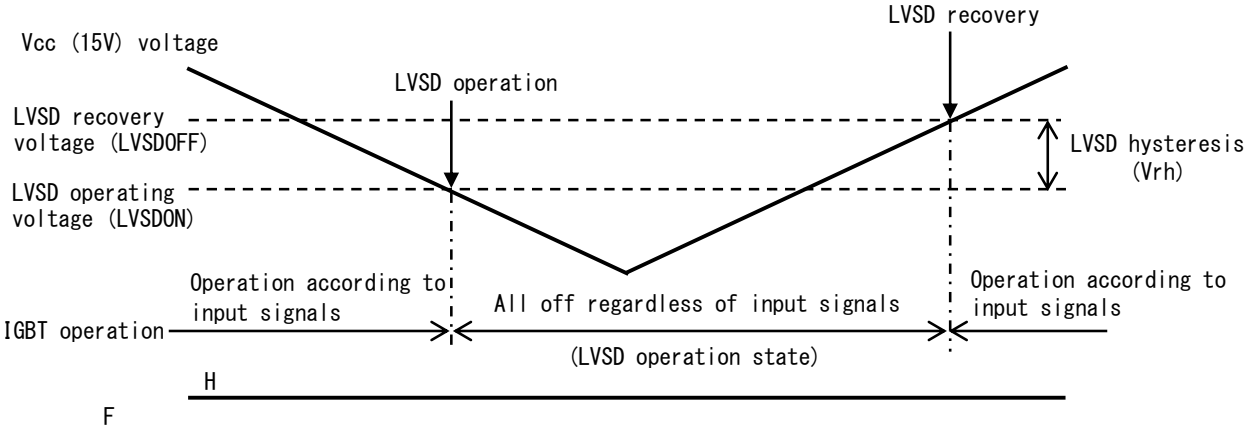


FIGURE 2.4.5.1 Timing Chart for Vcc Low-voltage Detection (LVSD Operation)

2.4.6 Over Temperature Protection

When the IC temperature exceeds the operating temperature of over temperature protection (TSDON), all IGBTs (top and bottom arms) are turned off. When the IC temperature goes down the hysteresis (TSDHYS) from the operating temperature of over temperature protection (TSDON), the IC returns to the state in which the IGBTs operate depending on input signals. “L” is not outputted to the F pin in this function operation.

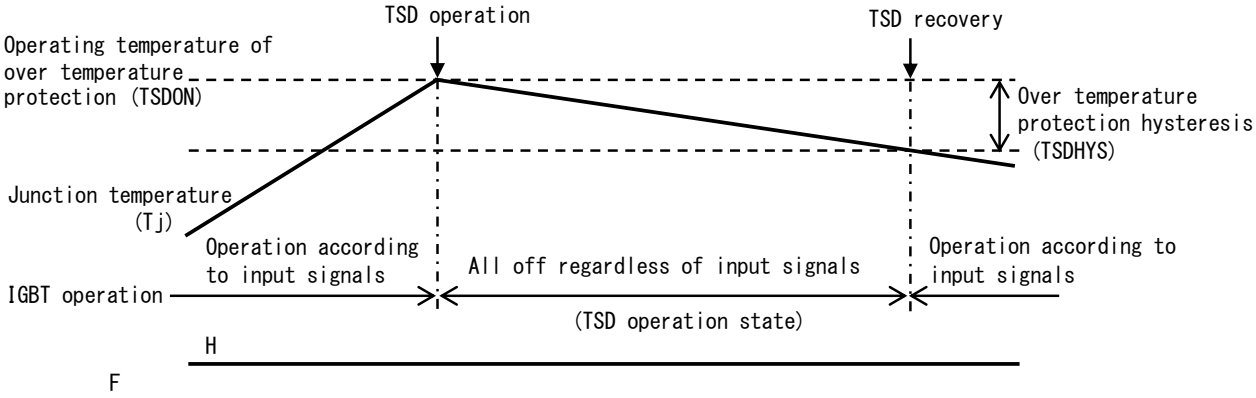


FIGURE 2.4.6.1 Timing Chart for Over Temperature Protection Operation

3. Standard Applications

3.1 External Components

TABLE 3.1.1 External Components

Component	Standard value	Usage	Remark
CH0, CL0	1.0μF±10%, 25V	Smooths the internal power supply (VB)	
CV1	1μF±10%, 25V	Smooths the Vcc power supply	Note 1
CV2	33nF±10%, 630V	Smooths the Vs power supply	Note 1
C1, C2	0.22μF±10%, 25V	For charge pump	Note 2
Rs	1Ω±1%, 1W	Sets current limit and over-current protection	Note 3 for how to set Rs.
RFU, RFV, RFW	10kΩ±5%	For pull up	
CF	0.01μF±10%, 25V	Eliminates output noise of Fault signal	In the case of OC=GL or CBH
RF	10kΩ±10%	For pull up	
CF	1000pF±10%, 25V	Sets over-current protection reset time	In the case of OC=VCC
RF	820kΩ±10%		

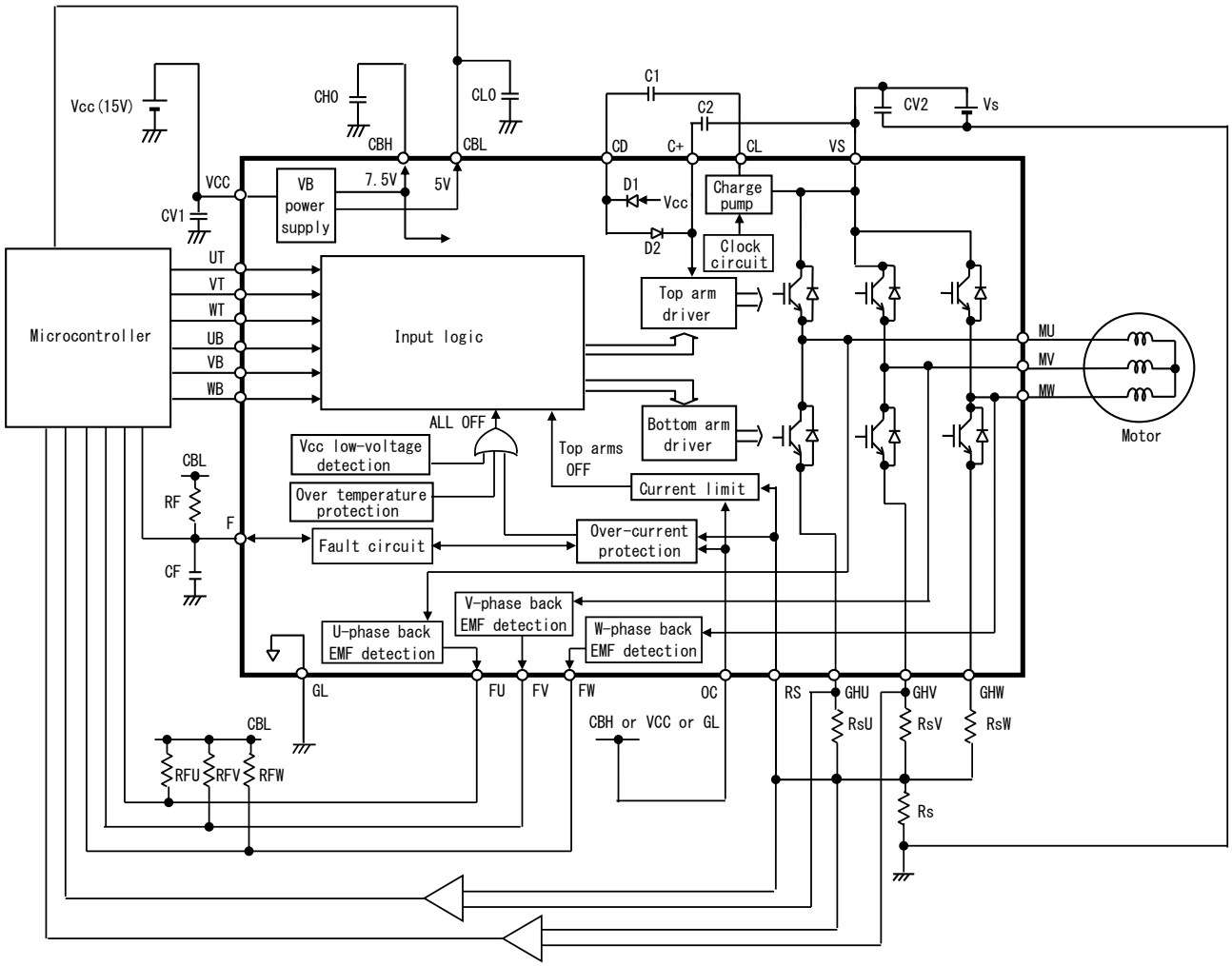


FIGURE 3.1.1 Block Diagram (ECN30622S is shown inside the bold line.)

Note 1. Caution for smoothing capacitor

As necessary, increase the capacitance and add a zener diode in consideration of noise immunity.

Note 2. Attention of component settings of charge pump circuit

When capacity of a capacitor is small, the voltage between the C+ pin and the VS pin drops because of the internal dissipation current from the C+ pin of the IC.

When the voltage between the C+ pin and the VS pin drops, the gate voltage of the top arm IGBTs also drops. The drop of the gate voltage could cause a rise of Tj because of ON-resistance increase of the top arm IGBTs and could cause a decrease in saturation current of the top arm IGBTs. That could lead to degradation or destruction of the IC. Caution is therefore needed when deciding capacity of a capacitor.

The voltage impressed to the capacitor is almost the same as Vcc in operation. Therefore, the withstand voltage of the capacitor requires more than the Vcc voltage. Pay close attention when using components other than those shown in TABLE 3.1.1.

Note 3. Caution for Rs resistance setting

The current limit set value (IO_1) can be calculated as follows.

IO_1 = Vref1/Rs

Vref1: Current limit reference voltage
Rs : Shunt resistance value

The over-current protection set value (IO_2) can be calculated as follows.

IO_2 = Vref2/Rs

Vref2: Over current protection reference voltage
Rs : Shunt resistance value

Delay time to turn output IGBT off (Tref1, Tref2) and variability of Vref1, Vref2, Rs need to be considered. Observe the output currents of the IC (the coil currents of the motor) and confirm a design margin.

When shunt resistance value is set, GHU, GHV, and GHW voltages are not allowed to exceed the range of GH voltage (Vgh).

3.2 Input Pins (UT, VT, WT, UB, VB, WB)

In some applications, input pins may be sensitive to noise due to high impedance. If noise is detected at an input pin, the following resistor and/or capacitor should be added.

- Resistor : 5.6kΩ ± 5% pull-down resistor between the GL pin and input pins
- Capacitor : 470pF ± 20% ceramic capacitor close to the input pin

4. Safe Operation Area (SOA) and Derating

4.1 Safe Operation Area (SOA)

The current and voltage at output pins must not be outside the SOA shown in FIGURE 4.1.1.

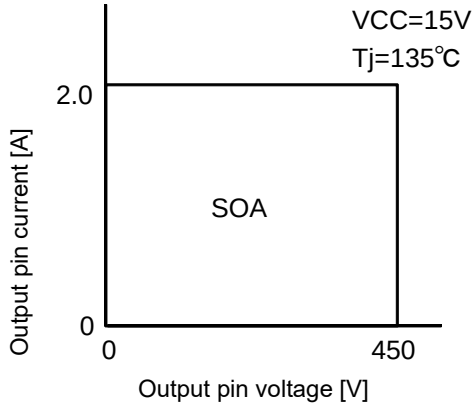


FIGURE 4.1.1 SOA

4.2 Shunt Resistor (Rs) Setting

Delay time to turn output IGBT off (Tref1, Tref2) and variability of Vref1, Vref2, Rs need to be considered, and the current must be below the derating curve of FIGURE 4.1.1.

4.3 General Design Derating Standards

(a) Temperature - Junction operating temperature must be kept under 110°C.
(b) Supply voltage - Vs power supply voltage must be kept under 450V.

Junction operating temperature depends on various parameters such as power supply voltages, ambient temperature, load, heat dissipation routes. Test it sufficiently by using actual systems.

5. Pin Locations

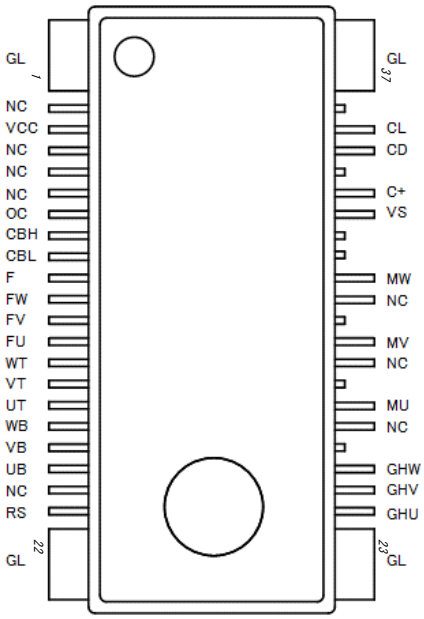


FIGURE 5.1 Pin Locations (Top view)

6. Explanations of Pins

TABLE 6.1 Explanations of Pins

Pin No.	Symbol	Explanation	Remark
1,22,23,37	GL	Ground	
2,4,5,6,20 27,29,31	NC	No connection	Note 2
3	VCC	15V power supply	
7	OC	Setting for current limit function (enable / disable) and over-current protection reset method	
8	CBH	VBH power supply output (7.5V)	
9	CBL	VBL power supply output (5V)	
10	F	Fault signal output or setting over-current protection reset time	
11	FW	W-phase back EMF signal output	
12	FV	V-phase back EMF signal output	
13	FU	U-phase back EMF signal output	
14	WT	Input control signal for W-phase top arm	
15	VT	Input control signal for V-phase top arm	
16	UT	Input control signal for U-phase top arm	
17	WB	Input control signal for W-phase bottom arm	
18	VB	Input control signal for V-phase bottom arm	
19	UB	Input control signal for U-phase bottom arm	
21	RS	Input for current limit and over-current protection	
24	GHU	Emitter of U-phase bottom arm IGBT and anode of U-phase bottom arm FWD	
25	GHV	Emitter of V-phase bottom arm IGBT and anode of V-phase bottom arm FWD	
26	GHW	Emitter of W-phase bottom arm IGBT and anode of W-phase bottom arm FWD	
28	MU	U phase output	Note 1
30	MV	V phase output	Note 1
32	MW	W phase output	Note 1
33	VS	High voltage power supply	Note 1
34	C+	For the charge pump circuit	Note 1
35	CD	For the charge pump circuit	Note 1
36	CL	For the charge pump circuit	Note 1

Note 1: High voltage pin. The voltage between CD and CL and between C+ and VS are low. Therefore, the distances between these pins are the same as those between low voltage pins.

Note 2: Not connected to the chip in the IC.

7. Inspection

Hundred percent inspection shall be conducted on electric characteristics at room temperature. For the operating temperature and hysteresis of the over temperature protection, equivalent inspections are conducted at room temperature.

8. Precautions for Use

8.1 Countermeasures against Electrostatic Discharge (ESD)

(a) Customers need to take precautions to protect ICs from electrostatic discharge (ESD). The material of the container or any other device used to carry ICs should be free from ESD, which can be caused by vibration during transportation. Use of electrically conductive containers is recommended as an effective countermeasure.

(b) Everything that touches ICs, such as the work platform, machine, measuring equipment, and test equipment, should be grounded.

(c) Workers should be high-impedance grounded (100kΩ to 1MΩ) while working with ICs, to avoid damaging the ICs by ESD.

(d) Friction with other materials, such as high polymers, should be avoided.

(e) When carrying a PCB with a mounted IC, ensure that the electric potential is maintained at a constant level using the short-circuit terminals and that there is no vibration or friction.

(f) The humidity at an assembly line where ICs are mounted on circuit boards should be kept around 45 to 75 percent using humidifiers or such. If the humidity cannot be controlled effectively, using ionized air blowers (ionizers) is effective.

8.2 Output Short-circuit Protection

This IC (the product of Hitachi Power Semiconductor Device, hereinafter called “HPSD’s IC”) could break by a short circuit (ex. load short). Therefore, external protection is needed.

8.3 Maximum Ratings

Regardless of changes in external conditions during use of HPSD’s IC, the “maximum ratings” described in this document should never be exceeded when designing electronic circuits that employ HPSD’s IC. If maximum ratings are exceeded, HPSD’s IC may be damaged or destroyed. In no event shall Hitachi Power Semiconductor Device (hereinafter called “HPSD”) be liable for any failure in HPSD’s IC or any secondary damage resulting from use at a value exceeding the maximum ratings.

8.4 Derating Design

Continuous high-load operation (high temperatures, high voltages, large currents) should be avoided and derating design should be applied, even within the ranges of the maximum ratings, to ensure reliability.

8.5 Safe Design

The HPSD’s IC may fail due to accidents or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy and measures to prevent misuse, in order to avoid extensive damage in the event of a failure.

8.6 Application

If HPSD’s IC is applied to the following uses where high reliability is required, obtain the document of permission from HPSD in advance.

・Automobile, Train, Vessel, etc.

Do not apply HPSD’s IC to the following uses where extremely high reliability is required.

・Nuclear power control system, Aerospace instrument, Life-support-related medical equipment, etc.

8.7 Soldering

(1) Soldering Condition

The recommended reflow soldering condition is shown in FIGURE 8.7.1.

High stress by mounting, such as long time thermal stress by preheating, mechanical stress, etc., can lead to degradation or destruction. Make sure that your mounting method does not cause problem as a system.

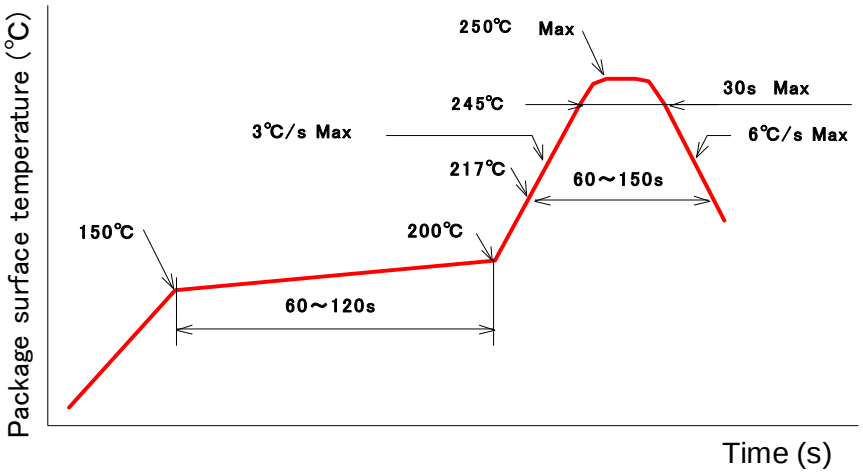


FIGURE 8.7.1 Recommended Conditions for Infrared Reflow or Air Reflow

(2) Reliability of Solder Connection

The reliability of solder connection depends on soldering condition, materials of circuit boards, footprint, etc. Test it sufficiently by heat cycle test, heat shock test, and so on after mounting ICs on circuit boards.

8.8 Storage Conditions

(1) Before opening the moisture prevention bag (aluminum laminate bag)

Temperature: 5 to 35℃
Humidity: less than 85%RH
Period: less than 2 years

(2) After opening the moisture prevention bag (aluminum laminate bag)

Temperature: 5 to 30℃
Humidity: less than 70%RH
Period: less than 1 week (from opening the bag to reflow soldering)

(3) Temporal storage after opening the moisture prevention bag

When ICs are stored temporarily after opening the bag they should be returned into the bag with desiccant within 10 minutes. Then, the open side of the bag should be folded under twice and closed with adhesive tape. And they should be kept in the following conditions.

Temperature: 5 to 35℃
Humidity: less than 85%RH
Period: less than 1 month

※ When the period of (1) to (3) is expected to expire, it is recommended to store the IC in a drying furnace (30%RH or lower) at ordinary temperature.

(4) Baking process

When the period of (1) to (3) has expired, the IC should be baked in accordance with the following conditions. (However, when the IC is stored in a drying furnace (30%RH or lower) at ordinary temperature, there is no need to bake.) Do not bake the tape and the reel of the taping package because they are not heat resistant. Transfer the IC to a heat resistant container prior to baking.

Temperature: 125±5℃
Period: 16 to 24 hours

8.9 Others

See “Instructions for Use of Hitachi High-Voltage Monolithic ICs” and “Application Note” for other precautions and instructions on how to deal with these kinds of products.

9. Usage

(1) HPSD warrants that the HPSD products have the specified performance according to the respective specifications at the time of its sale. Testing and other quality control techniques of the HPSD products by HPSD are utilized to the extent HPSD needs to meet the specifications described in this document. Not every device of the HPSD products is specifically tested on all parameters, except those mandated by relevant laws and/or regulations.

(2) Following any claim regarding the failure of a product to meet the performance described in this document made within one month of product delivery, all the products in relevant lot(s) shall be re-tested and re-delivered. The HPSD products delivered more than one month before such a claim shall not be counted for such response.

(3) HPSD assumes no obligation nor makes any promise of compensation for any fault which should be found in a customer's goods incorporating the products in the market. If a product failure occurs for reasons obviously attributable to HPSD and a claim is made within six months of product delivery, HPSD shall offer free replacement or payment of compensation. The maximum compensation shall be the amount paid for the products, and HPSD shall not assume responsibility for any other compensation.

(4) HPSD reserves the right to make changes in this document and to discontinue mass production of the relevant products without notice. Customers are advised to confirm specification of the product of inquiry before purchasing of the products that the customer desired. Customers are further advised to confirm before purchasing of such above products that the product of inquiry is the latest version and that the relevant product is in mass production status if the purchasing of the products by the customer is suspended for one year or more.

(5) When you dispose of HPSD products and/or packing materials, comply with the laws and regulations of each country and/or local government. Conduct careful preliminary studies about environmental laws applying to your products such as RoHS, REACH. HPSD shall not assume responsibility for compensation due to contravention of laws and/or regulations.

(6) HPSD shall not be held liable in any way for damages and infringement of patent rights, copyright or other intellectual property rights arising from or related to the use of the information, products, and circuits in this document.

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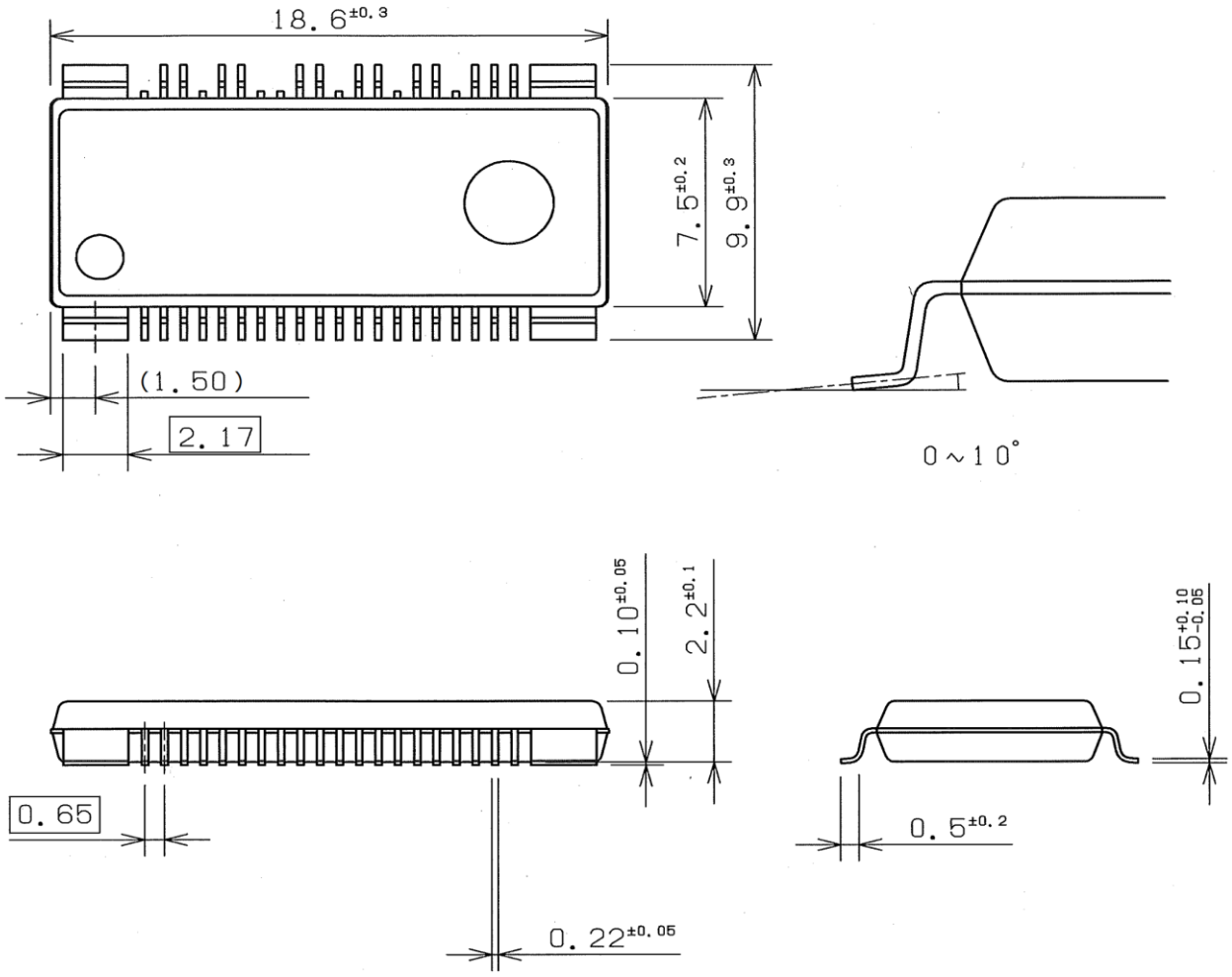
(9) You shall not use the HPSD products (technologies) described in this document and any other products (technologies) manufactured or developed by using them (hereinafter called "END Products") or supply the HPSD products (technologies) and END Products for the purpose of disturbing international peace and safety, including (ⅰ) the design, development, production, stockpiling or any use of weapons of mass destruction such as nuclear, chemical or biological weapons or missiles, (ⅱ) the other military activities, or (ⅲ) any use supporting these activities. You shall not sell, export, dispose of, license, rent, transfer, disclose or otherwise provide the HPSD products (technologies) and END Products to any third party whether directly or indirectly with knowledge or reason to know that the third party or any other party will engage in the activities described above.
When exporting, re-export transshipping or otherwise transferring the HPSD products (technologies) and END Products, all necessary procedures are to be taken in accordance with Foreign Exchange and Foreign Trade Act (Foreign Exchange Act) of Japan, Export Administration Regulations (EAR) of US, and any other applicable export control laws and regulations promulgated and administered by the governments of the countries asserting jurisdictions over the parties or transaction.

◆Appendix - Supplementary Data

1. Dimensions



Unit: mm

FIGURE A: Dimensions

2. External Packaging

FIGURE B shows the external packaging. Order quantities are basically multiples of 2000.

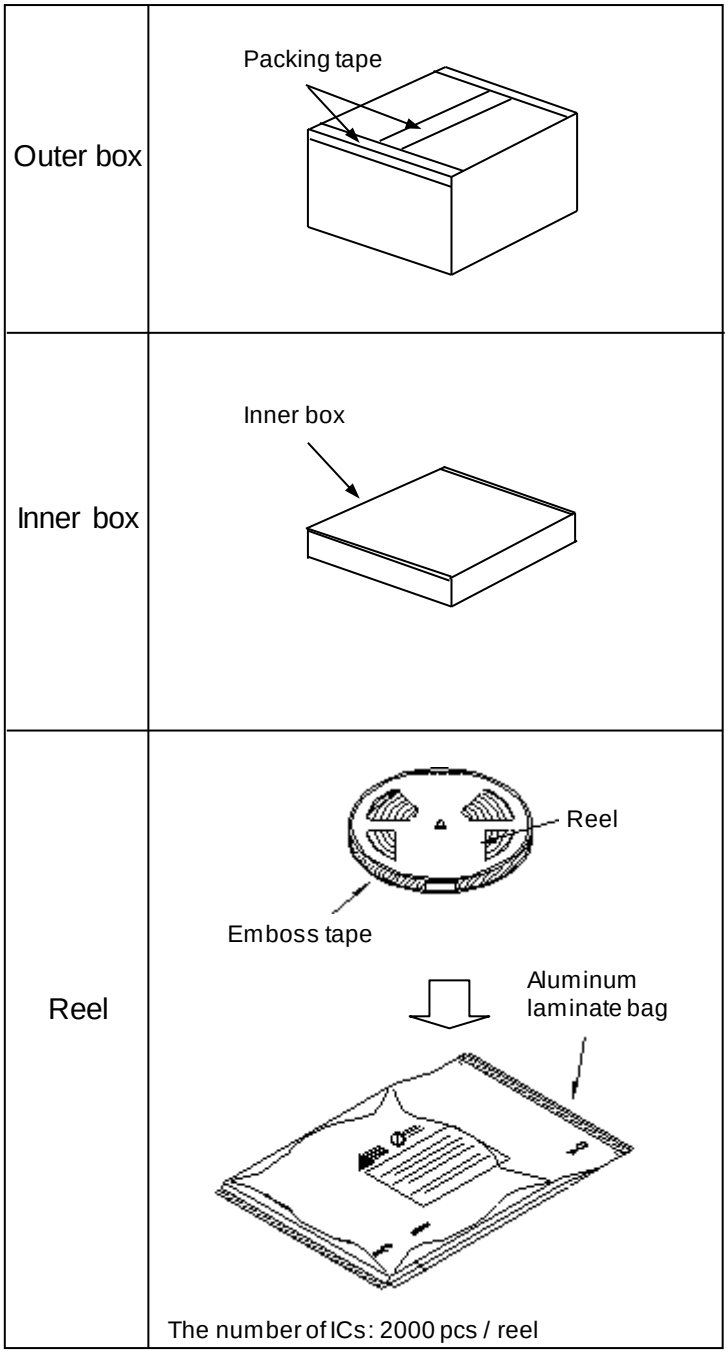


FIGURE B: External Packaging

Precautions for Safe Use and Notices

If semiconductor devices are handled in an inappropriate manner, failures may result. For this reason, be sure to read the latest version of “Instructions for Use of Hitachi High-Voltage Monolithic ICs” before use.

This mark indicates an item requiring caution.

CAUTION This mark indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury and damage to property.

CAUTION

(1) Regardless of changes in external conditions during use of semiconductor devices, the “maximum ratings” and “safe operating area(SOA)” should never be exceeded when designing electronic circuits that employ semiconductor devices.

(2) Semiconductor devices may fail due to accidents or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy and measures to prevent misuse, in order to avoid extensive damage in the event of a failure.

(3) If semiconductor devices are applied to uses where high reliability is required, obtain the document of permission from HPSD in advance (Automobile, Train, Vessel, etc.). Do not apply semiconductor devices to uses where extremely high reliability is required (Nuclear power control system, Aerospace instrument, Life-support-related medical equipment, etc.).

(If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

NOTICES

1. This Data Sheet contains the specifications, characteristics, etc. concerning power semiconductor products (hereinafter called “products”).
2. All information included in this document such as product data, diagrams, charts, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, specifications of products, etc. are subject to change without prior notice. Before purchasing or using any of the HPSD products listed in this document, please confirm the latest product information with a HPSD sales office.
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   When exporting, re-export transshipping or otherwise transferring the HPSD products (technologies) and END Products, all necessary procedures are to be taken in accordance with Foreign Exchange and Foreign Trade Act (Foreign Exchange Act) of Japan, Export Administration Regulations (EAR) of US, and any other applicable export control laws and regulations promulgated and administered by the governments of the countries asserting jurisdictions over the parties or transaction.
7. In no event shall HPSD be liable for any failure in HPSD products or any secondary damage resulting from use at a value exceeding the maximum ratings.

Refer to the following website for the latest information. Contact a HPSD sales office if you have any questions.

http://www.hitachi-power-semiconductor-device.co.jp/en/