16-channel High Voltage analog switch IC

ECN32910TF/32911TF Product Specification

1. General Description

1.1 General

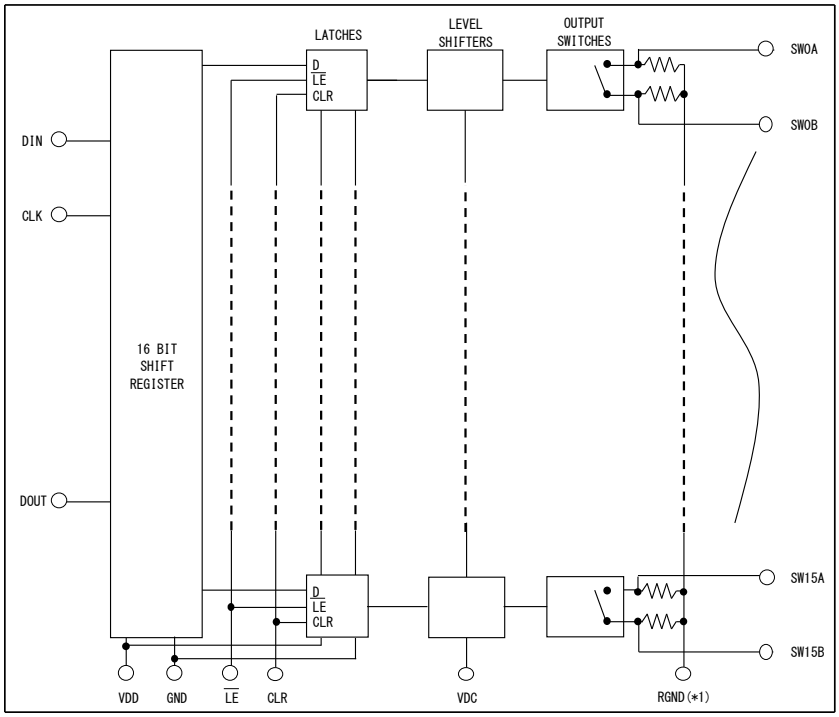
ECN32910TF/32911TF are 16-channel High Voltage analog switching IC on which latch-up free is realized by SOI isolation technology.

High voltage and low on-resistance MOS switches are used as output devices controlled by a 3.3V or 5.0V signal. ECN32910/32911 is most suited to ultrasound imaging applications.

1.2 Functions and Features

* High voltage and low on-resistance MOS switches integrated.
* 16bit shift resister integrated.
* Integrated bleed resistors on the outputs.(ECN32911 only)
* Switch on-resistance: 18 Ω typ. (VDC=12V, ISIG=5mA, 25ºC)
* Switch breakdown voltage: 120V
* No dedicated high voltage power supplies are required.
* Low power consumption.
* 48-pin LQFP Package. (RoHS compliant)

1.3 Block diagram



(*1) ECN32911 integrates bleed resistors and has RGND terminal.

Fig. 1.3.1 Block diagram

2. Specifications

2.1 Absolute Maximum Ratings

Table 2.1.1 Absolute Maximum Ratings

No.	Items	Symbol	Terminal	Values	Unit	Note
1	Logic power supply voltage	VDD	VDD	-0.5 to +7.0	V	Ta＝25ºC
2	VDC voltage supply	VDC	VDC	-0.5 to 15.5	V	Ta＝25ºC
3	Logic input voltages	-	DIN,CLK,CLR, $\overline{LE}$	-0.5 to VDD+0.3	V	Ta＝25ºC
4	Analog signal range	-	SW0 to SW15	-120 to +120	V	Ta＝25ºC
5	Operating junction temperature	Tjop	-	-20 to +125	ºC	
6	Storage temperature	Tstg	-	-55 to +150	ºC	
7	Power dissipation	Pw	-	1.0	W	Ta＝70ºC

2.2 Electrical Characteristics

2.2.1 DC Characteristics

Table 2.2.1 DC Characteristics Ta=25°C VDC=12V VDD=5.0V

No.	Items	Symbol	Spec			Unit	Test conditions
			Min	Typ	Max		
1	Small signal switch on resistance	RONS	–	18	26	Ω	ISIG=5mA
			–	18	26		ISIG=200mA
2	Small signal switch on resistance matching	ΔRONS	–	5	20	%	ISIG=5mA
3	Large signal switch on resistance	RONL	–	16	–	Ω	ISIG=1A
4	Value of output bleed resistance	RINT	20	35	50	kΩ	IRINT=0.5mA, Output switch to RGND
5	Switch off leakage per switch	ISOL	–	1	10	μA	VSIG=100V
			–	1	3	mA	VSIG=-100V (32910)
			–	3	7	mA	VSIG=-100V (32911)
6	Switch cut off current	ISCC	–	1	10	μA	VSIG=100V or -100V
7	DC offset switch (off)	DCOFF	–	10	100	mV	RL=100kΩ (32910)
			–	10	100	mV	no-load (32911)
8	DC offset switch (on)	DCON	–	10	100	mV	RL=100kΩ (32910)
			–	10	100	mV	no-load (32911)
9	VDC average current	IDC	–	–	3	mA	fsw=50kHz, no-load
10	VDC quiescent current	IDCQ1	–	10	50	μA	All SWs off
		IDCQ2	–	10	50	μA	All SWs on, ISIG=5mA
11	VDC peak current	IDSC	–	–	7	mA	All SWs on, VSIG=-100V
12	VDD average current	IDD	–	–	3.0	mA	fCLK=5MHz
13	VDD quiescent current	IDDQ	–	–	10	μA	
14	Data out source current	ISOR	0.45	0.70	–	mA	Vdout=VDD-0.7V
15	Data out sink current	ISINK	0.45	0.70	–	mA	Vdout=0.7V

2.2.2 AC Characteristics

Table 2.2.2 AC Characteristics Ta=25°C VDC=12V VDD=5.0V

No.	Items	Symbol	Spec			Unit	Test conditions
			Min	Typ	Max		
1	SW Turn on time	tON	–	–	3.0	μs	VSIG=100V, RL=10kΩ
2	SW Turn off time	tOFF	–	–	3.0	μs	VSIG=100V, RL=10kΩ
3	Clock frequency	fCLK	–	–	30	MHz	50% duty cycle, fDIN=fCLK/2 VDD= 5.0V
			–	–	20	MHz	50% duty cycle, fDIN=fCLK/2 VDD=3.3V
4	Clock delay time to data out	tDO	–	–	48	ns	DOUT terminal, VDD=3.3V
			–	–	32	ns	DOUT terminal, VDD=5.0V

2.2.3 AC Characteristics (for reference purpose only)

These items are not tested when shipped.

Table 2.2.3 AC Characteristics (for reference purpose only) Ta=25°C VDC=12V VDD=5.0V

No.	Items	Symbol	Spec			Unit	Condition
			Min	Typ	Max		
1	Off capacitance SW to GND	CSG (off)	–	15	–	pF	Measurement signal (DC 0V, AC 1MHz)
2	On Capacitance SW to GND	CSG (on)	–	25	–	pF	Measurement signal (DC 0V, AC 1MHz)
3	SW off isolation	KO	-28	-32	–	dB	f=5MHz, RL=1kΩ//15pF
			-50	-54	–	dB	f=5MHz, RL=50Ω
4	SW crosstalk	KCR	-50	-54	–	dB	f=5MHz, RL=50Ω
5	Output voltage spike	+VSPK	–	–	40	mV	RL=50Ω
		-VSPK	-20	–	–		

3. Recommended Operating Conditions

Please operate in use within the limit of recommended operating conditions detailed in Table 3.1.

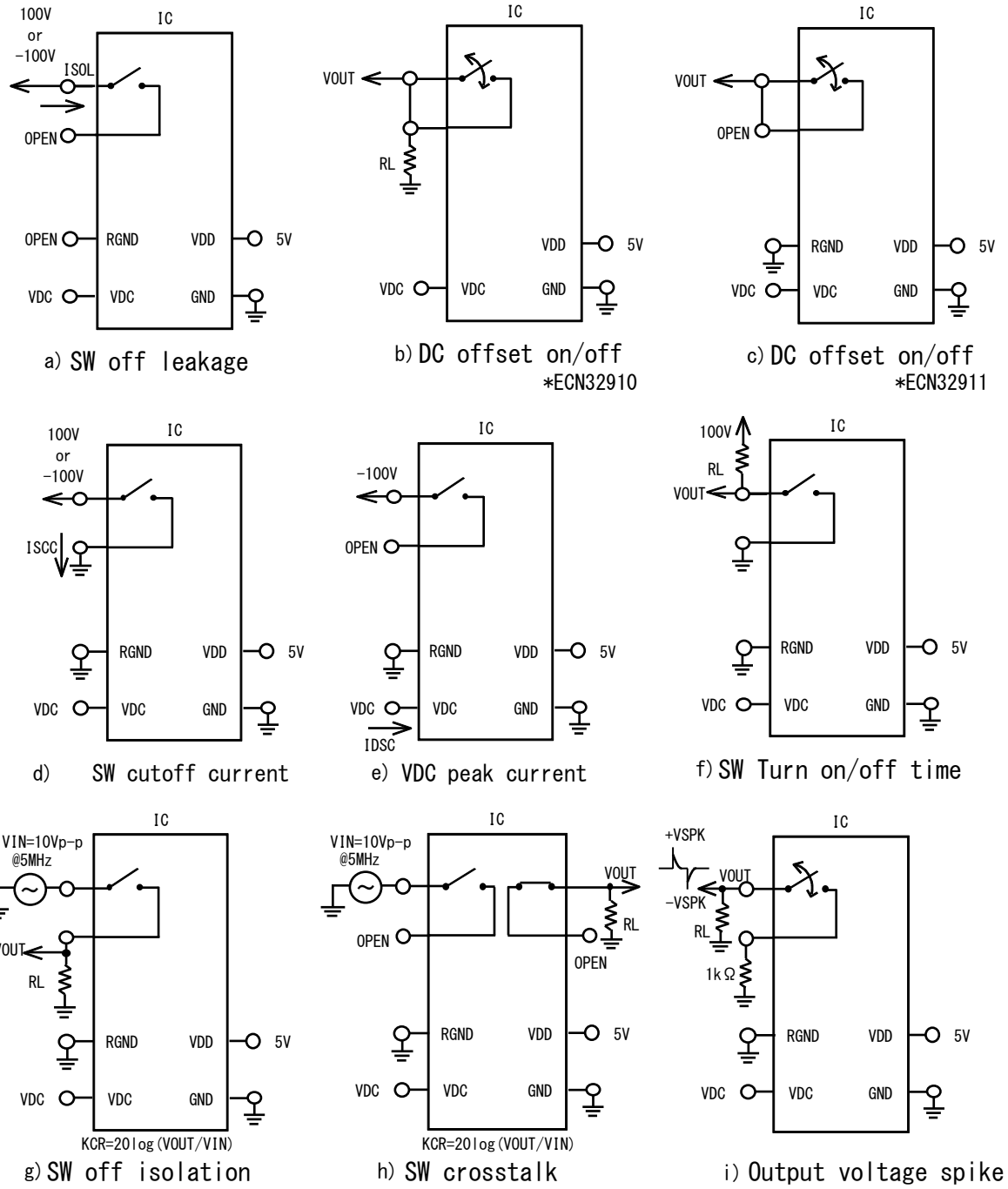
Table 3.1 Recommended Operating Conditions

No	Items	Symbol	Recommended Value	Unit	Condition
1	Logic power supply voltage	VDD	3.0 to 5.5	V	
2	VDC voltage supply	VDC	10 to 15	V	
3	High-level input voltage	VIH	0.9VDD to VDD	V	
4	Low-level input voltage	VIL	0 to 0.1VDD	V	
5	Analog signal voltage peak to peak	VSIG	-100 to 100	V	
6	Analog signal frequency	fsig	Min.100	kHz	
7	Operating free air-temperature	Ta	0 to 70	^{o}C	
8	Switching frequency	fSW	50 max	kHz	Duty Cycle=50%
9	Set up time for $\overline{LE}$	tSD	Min.60	ns	
10	Pulse width of $\overline{LE}$	tWLE	Min.40	ns	
11	Time width of CL	tWCL	Min.40	ns	
12	Set up time DATA to Clock	tSU	Min.10	ns	
13	Hold time DATA from Clock	th	Min.10	ns	
14	Maximum VSIG Slew Rate	dV/dt	Max.30	V/ ns	

Attention ;

1) GND terminal must be connected during power-up and power-down.
2) It is indispensable overshoot/undershoot voltage of power supplies(VDD, VDC) do NOT exceed maximum rated voltage in the event of power-up and power-down.

4. Test Circuit



Note.
RGND pin is N/C pin and is not connected in ECN32910.

Fig. 4.1 Test Circuit

5. Timing Waveforms

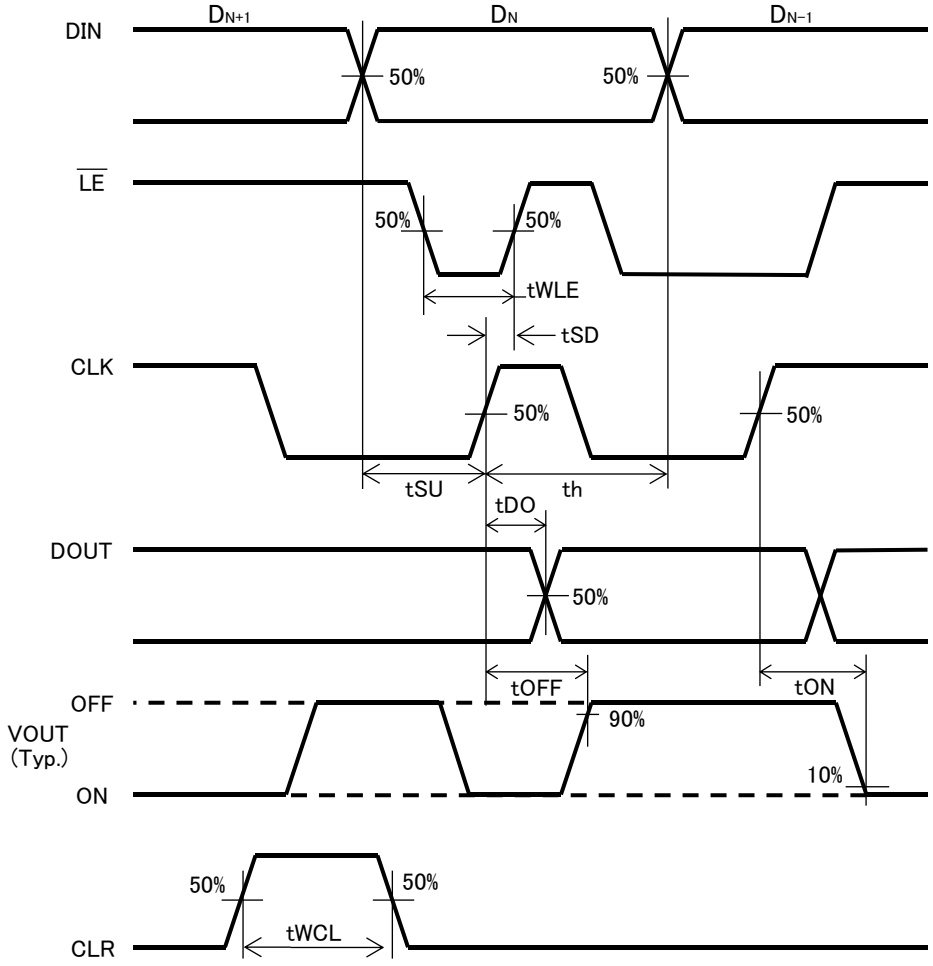


Fig. 5.1 Timing Waveforms

Note

1. Serial data is clocked in on the rising edge of CLK.

2. The switches go to a state retaining their present condition on the rising edge of LE.

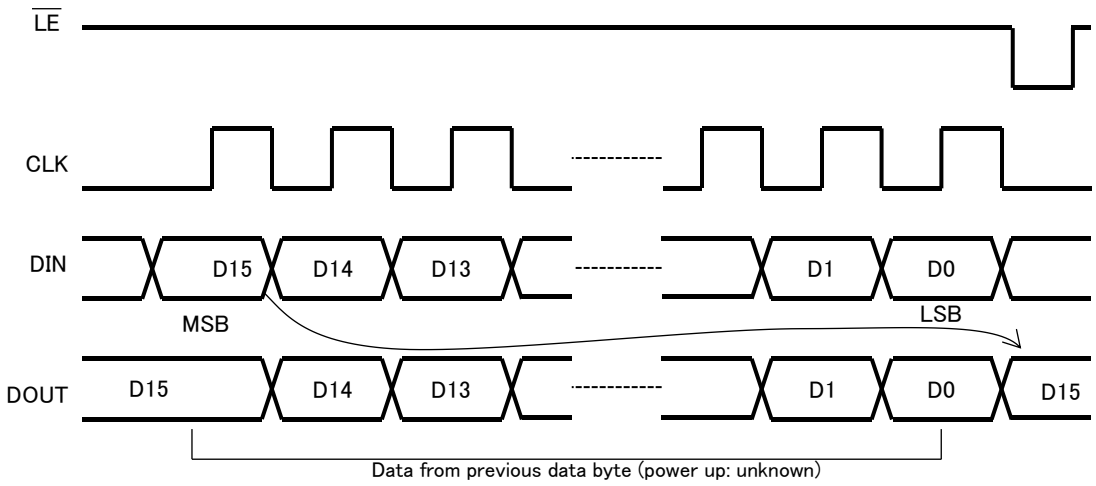


Fig. 5.2 LATCH ENABLE Timing waveforms

6. Truth Table

Table 6.1 Truth table

D0	D1	D2	D3	D4	D5	D6	D7	LE	CLR	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

D8	D9	D10	D11	D12	D13	D14	D15	$\overline{LE}$	CLR	SW8	SW9	SW10	SW11	SW12	SW13	SW14	SW15
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

X = Don't care

Note

1. The 16 Switches operate independently.

2. When $\overline{LE}$ is low, the shift register data flows through the latch.

3. Shift register clocking has no effect on the switch states if $\overline{LE}$ is high.

4. When switch 15 is ON, DOUT will be high.

5. The clear input overrides all other inputs.

7. Pin Function

ECN32910TF/32911TF LQFP48（48Pin LQFP）

Table 7.1 Pin Function

Pin	Name	Functions	Note
1	N/C	No connection	*1
2	N/C	No connection	*1
3	SW4B	Analog Switch 4	
4	SW4A	Analog Switch 4	
5	SW3B	Analog Switch 3	
6	SW3A	Analog Switch 3	
7	SW2B	Analog Switch 2	
8	SW2A	Analog Switch 2	
9	SW1B	Analog Switch 1	
10	SW1A	Analog Switch 1	
11	SW0B	Analog Switch 0	
12	SW0A	Analog Switch 0	
13	GND2	Ground	
14	N/C	No connection	*1
15	VDC	VDC voltage supply	
16	N/C	No connection	*1
17	GND	Ground	
18	VDD	Logic Supply Voltage	
19	DIN	Serial Data Input	
20	CLK	Serial Clock Input	
21	$\overline{LE}$	Latch-Enable Input	
22	CLR	Latch-Clear Input	
23	DOUT	Serial Data Output	
24	RGND(N/C)	Ground(ECN32911TF) / No connection(ECN32910TF)	*2
25	SW15B	Analog Switch 15	
26	SW15A	Analog Switch 15	
27	SW14B	Analog Switch 14	
28	SW14A	Analog Switch 14	
29	SW13B	Analog Switch 13	
30	SW13A	Analog Switch 13	
31	SW12B	Analog Switch 12	
32	SW12A	Analog Switch 12	
33	SW11B	Analog Switch 11	
34	SW11A	Analog Switch 11	
35	N/C	No connection	*1
36	N/C	No connection	*1
37	SW10B	Analog Switch 10	
38	SW10A	Analog Switch 10	
39	SW9B	Analog Switch 9	
40	SW9A	Analog Switch 9	
41	SW8B	Analog Switch 8	
42	SW8A	Analog Switch 8	
43	SW7B	Analog Switch 7	
44	SW7A	Analog Switch 7	
45	SW6B	Analog Switch 6	
46	SW6A	Analog Switch 6	
47	SW5B	Analog Switch 5	
48	SW5A	Analog Switch 5	

Note *1. NOT connected on chip internal.*
2. RGND terminal connects to bleed resistors on chip internal.(ECN32911TF only).

8. Pin configuration

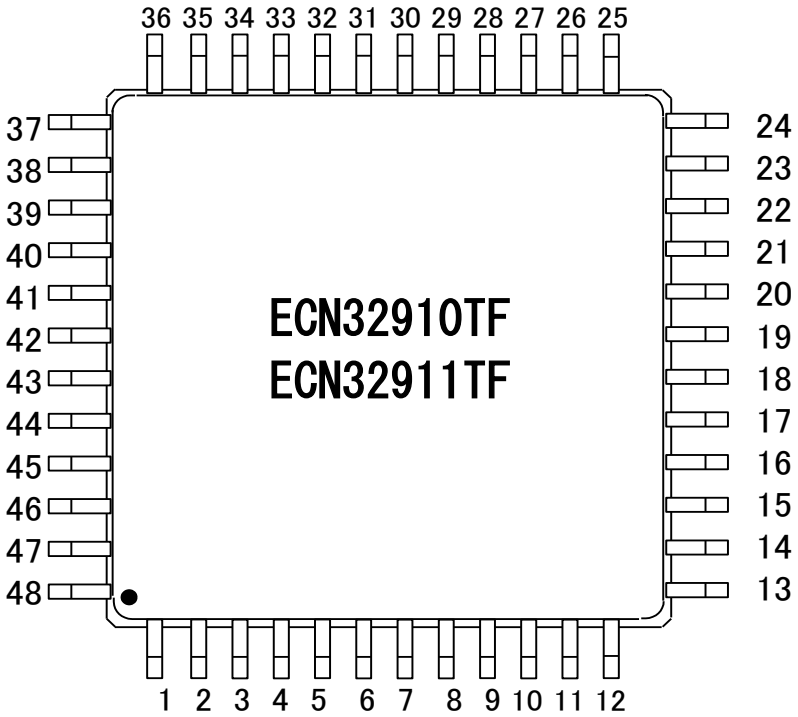


Fig. 8.1 Pin configuration(Top view)

9. Inspection

Hundred percent inspections shall be conducted on electric characteristics.

10. Precautions for use

10.1 Countermeasures against Electrostatic Discharge (ESD)

(a) Customers need to take precautions to protect ICs from electrostatic discharge (ESD). The material of the container or any other device used to carry ICs should be free from ESD, which can be caused by vibration during transportation. Use of electrically conductive containers is recommended as an effective countermeasure.

(b) Everything that touches ICs, such as the work platform, machine, measuring equipment, and test equipment, should be grounded.

(c) Workers should be high-impedance grounded (100kΩ to 1MΩ) while working with ICs, to avoid damaging the ICs by ESD.

(d) Friction with other materials, such as high polymers, should be avoided.

(e) When carrying a PCB with a mounted IC, ensure that the electric potential is maintained at a constant level using the short-circuit terminals and that there is no vibration or friction.

(f) The humidity at an assembly line where ICs are mounted on circuit boards should be kept around 45 to 75 percent using humidifiers or such. If the humidity cannot be controlled effectively, using ionized air blowers (ionizers) is effective.

10.2 Output Short-circuit Protection

This IC (the product of Hitachi Power Semiconductor Device, hereinafter called “HPSD’s IC”) could break by a short circuit (ex. load short). Therefore, external protection is needed.

10.3 Maximum Ratings

Regardless of changes in external conditions during use of HPSD’s IC, the “maximum ratings” described in this document should never be exceeded when designing electronic circuits that employ HPSD’s IC. If maximum ratings are exceeded, HPSD’s IC may be damaged or destroyed. In no event shall Hitachi Power Semiconductor Device (hereinafter called “HPSD”) be liable for any failure in HPSD’s IC or any secondary damage resulting from use at a value exceeding the maximum ratings.

10.4 Derating Design

Continuous high-load operation (high temperatures, high voltages, large currents) should be avoided and derating design should be applied, even within the ranges of the maximum ratings, to ensure reliability.

10.5 Safe Design

The HPSD’s IC may fail due to accidents or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy and measures to prevent misuse, in order to avoid extensive damage in the event of a failure.

10.6 Application

If HPSD’s IC is applied to the following uses where high reliability is required, obtain the document of permission from HPSD in advance.

・Automobile, Train, Vessel, etc.

Do not apply HPSD’s IC to the following uses where extremely high reliability is required.

・Nuclear power control system, Aerospace instrument, Life-support-related medical equipment, etc.

10.7 Soldering

Lead-free solder is used for coating pins and the tab of this IC.

Refer to "Precautions for Use of High Voltage Monolithic Ics” for soldering conditions.

10.8 Storage Conditions

(1) Before opening the moisture prevention bag (aluminum laminate bag)

Temperature: less than 40℃
Humidity: less than 90%RH
Period: less than 12 months

(2) After opening the moisture prevention bag (aluminum laminate bag)

Temperature: 5℃ to 30℃
Humidity: less than 60%RH
Period: less than 168 hours

※ When the period of (1) and (2) is likely to expire, store the IC in a drying furnace (10%RH or lower) at ordinary temperature.

(3) Baking process

When the period of (1) and (2) has expired, the IC should be baked in accordance with the following conditions. (However, when the IC is stored in a drying furnace (10%RH or lower) ordinary temperature, there is no need to bake.) Do not bake the tape and the reel of the taping package because they are not heat resistant. Transfer the IC to a heat resistant container prior to baking.

Temperature: 125℃ to 135℃
Period: more than 48 hours

10.9 Others

See “Instructions for Use of Hitachi High-Voltage Monolithic ICs” for other precautions and instructions on how to deal with these kinds of products.

11. Usage

(1) HPSD warrants that the HPSD products have the specified performance according to the respective specifications at the time of its sale. Testing and other quality control techniques of the HPSD products by HPSD are utilized to the extent HPSD needs to meet the specifications described in this document. Not every device of the HPSD products is specifically tested on all parameters, except those mandated by relevant laws and/or regulations.

(2) Following any claim regarding the failure of a product to meet the performance described in this document made within one month of product delivery, all the products in relevant lot(s) shall be re-tested and re-delivered. The HPSD products delivered more than one month before such a claim shall not be counted for such response.

(3) HPSD assumes no obligation nor makes any promise of compensation for any fault which should be found in a customer's goods incorporating the products in the market. If a product failure occurs for reasons obviously attributable to HPSD and a claim is made within six months of product delivery, HPSD shall offer free replacement or payment of compensation. The maximum compensation shall be the amount paid for the products, and HPSD shall not assume responsibility for any other compensation.

(4) HPSD reserves the right to make changes in this document and to discontinue mass production of the relevant products without notice. Customers are advised to confirm specification of the product of inquiry before purchasing of the products that the customer desired. Customers are further advised to confirm before purchasing of such above products that the product of inquiry is the latest version and that the relevant product is in mass production status if the purchasing of the products by the customer is suspended for one year or more.

(5) When you dispose of HPSD products and/or packing materials, comply with the laws and regulations of each country and/or local government. Conduct careful preliminary studies about environmental laws applying to your products such as RoHS, REACH. HPSD shall not assume responsibility for compensation due to contravention of laws and/or regulations.

(6) HPSD shall not be held liable in any way for damages and infringement of patent rights, copyright or other intellectual property rights arising from or related to the use of the information, products, and circuits in this document.

(7) No license is granted by this document of any patents, copyright or other intellectual property rights of any third party or of HPSD.

(8) This document may not be reprinted, reproduced or duplicated, in any form, in whole or in part without the express written permission of HPSD.

(9) You shall not use the HPSD products (technologies) described in this document and any other products (technologies) manufactured or developed by using them (hereinafter called "END Products") or supply the HPSD products (technologies) and END Products for the purpose of disturbing international peace and safety, including (i) the design, development, production, stockpiling or any use of weapons of mass destruction such as nuclear, chemical or biological weapons or missiles, (ii) the other military activities, or (iii) any use supporting these activities. You shall not sell, export, dispose of, license, rent, transfer, disclose or otherwise provide the HPSD products (technologies) and END Products to any third party whether directly or indirectly with knowledge or reason to know that the third party or any other party will engage in the activities described above.
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◆Appendix-Supplementary Data

1. Package Outline

Units : mm

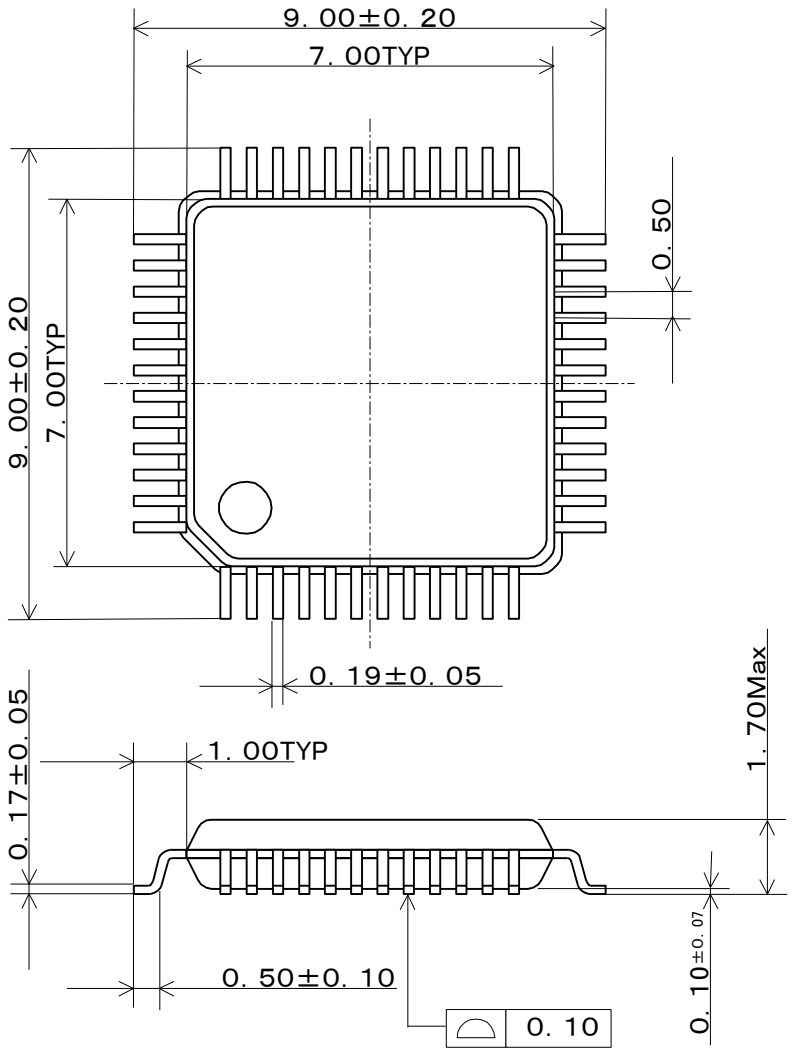


Fig.A Package outline

2. Marking spec

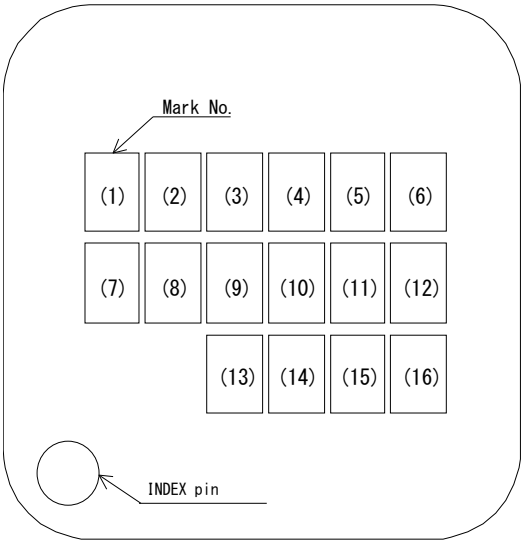


Fig.B Marking

1) No.(1) ; Blank

2) No.(2)～(6) ; Manufacturing No.
No.(2) ; Year code (Least significant digit of Assembled year (A.D.))
No.(3) ; Month code (Refer to below.)
Jan. ; A, Feb. ; B, Mar. ; C, Apr, ; D,
May ; E, June ; K, July ; L, Aug. ; M,
Sep. ; N, Oct. ; X, Nov. ; Y, Dec. ; Z
No.(4)～(6) ; Serial number

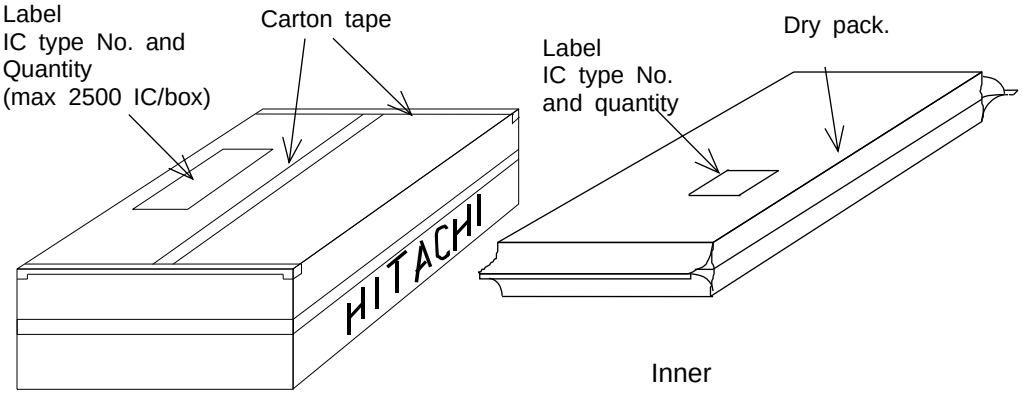
3) No.(7) ; Blank

4) No.(8)～(16) ; Product name ; ECN32910TF or ECN32911TF

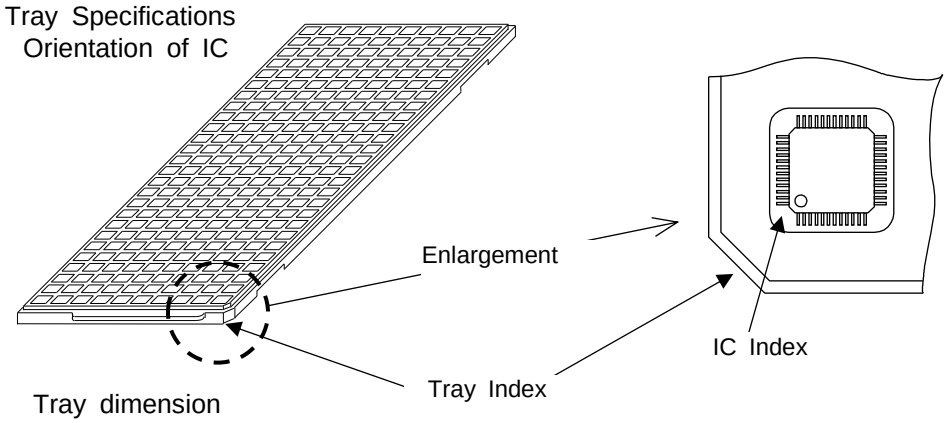
3. Packing Form

Packaging details are as shown below.

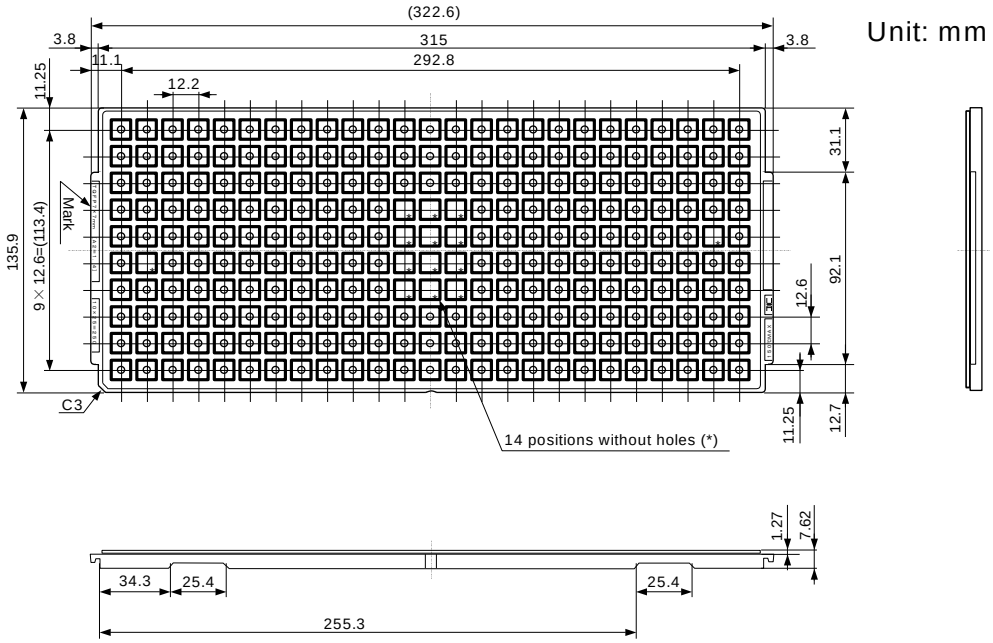
1.Outer and inner packing



2.Tray



Tray dimension



Unit: mm

(1) Material of tray is PPE containing carbon and static proof.
(2) Packing quantity is max 250 IC/Tray.
(3) Maximum heat resistant temperature is 150deg.

Fig.C IC packing detail

4. Function Description

Please read below contents before using this product.

(1) Function Description

・Bleed resistor

ECN32911TF has integrated 35kΩ bleed resistor to discharge capacitive Loads such as piezoelectric transducers. Each analog switch terminal is connected RGND with a bleed resistor.

・Power supply sequence free

ECN32910TF/32911TF doesn't require the power up/down special sequence of the VDC and VDD power supplies.
However, shift register and latch are unsettled just after power-up.
Therefore, it's necessary to set the data of shift register after power-up.
(Please refer to the truth table. : Table.6.1)

(2) Analog signal range

Analog signal frequency must be greater than 100KHz with less than 50% duty cycle when VSIG >10Vp-p.
There is no limited for analog signal frequency and switches can transmit DC, burst and continuous wave(CW) signal when VSIG <10Vp-p.

Precautions for Safe Use and Notices

If semiconductor devices are handled in an inappropriate manner, failures may result. For this reason, be sure to read the latest version of “Instructions for Use of Hitachi High-Voltage Monolithic ICs” before use.

This mark indicates an item requiring caution.

CAUTION This mark indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury and damage to property.

CAUTION

(1) Regardless of changes in external conditions during use of semiconductor devices, the “maximum ratings” and “safe operating area(SOA)” should never be exceeded when designing electronic circuits that employ semiconductor devices.

(2) Semiconductor devices may fail due to accidents or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy and measures to prevent misuse, in order to avoid extensive damage in the event of a failure.

(3) If semiconductor devices are applied to uses where high reliability is required, obtain the document of permission from HPSD in advance (Automobile, Train, Vessel, etc.). Do not apply semiconductor devices to uses where extremely high reliability is required (Nuclear power control system, Aerospace instrument, Life-support-related medical equipment, etc.).

(If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

NOTICES

1. This Data Sheet contains the specifications, characteristics, etc. concerning power semiconductor products (hereinafter called “products”).
2. All information included in this document such as product data, diagrams, charts, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, specifications of products, etc. are subject to change without prior notice. Before purchasing or using any of the HPSD products listed in this document, please confirm the latest product information with a HPSD sales office.
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