16-chanel High Voltage analog switch IC

ECN32910FN/32911FN Product Specification Rev. 3

ECN32910FN/32911FN is 16-channel High Voltage analog switching IC on which latch-up free is realized by SOI isolation technology.

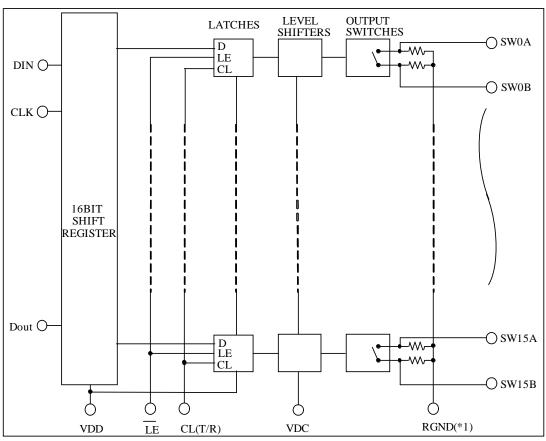
High voltage and low ON-resistance MOS switches are used as output devices controlled by a 3.3V or 5V signal. ECN32910/32911 is the most suited to Ultrasound Imaging applications.

Functions

- * High voltage and low on-resistance MOS switches are integrated.
- * Integrated 16bit shift resister
- * Integrated bleed resistors on the outputs.(ECN32911FN only)

Features

- * No high voltage power supply required
- * Low power consumption
- * Switch on-resistance: 18 Ω typ. (ISIG=5mA, 25°C)
- * Switch breakdown voltage: 120V
- * 48-pin WQFN Package (RoHS compliant)



(*1) ECN32911 integrates bleed resistors which are connected to RGND terminal on internal IC

Fig.1 Block diagram

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1. General

This Specification shall be applied to the following semiconductor integrated circuit.

1) Parts name: ECN32910FN/32911FN

2) Application : Ultrasound imaging scanner and others

3) Structure : Monolithic IC 4) Package : WQFN48

2. Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings

No.	Items	Symbol Terminal		Values	Unit	Note
1	Logic power supply voltage	VDD	VDD	-0.5 to +7.0	V	Ta=25°C
2	VDC voltage supply	VDC	VDC	-0.5 to 15.5	V	Ta=25°C
3	Logic input voltages	VIN	DIN, CLK,CL, LE	-0.5 to VDD+0.3	>	Ta=25°C
4	Analog signal range	-	SW0 to SW15	-120 to +120	V	Ta=25°C
5	Operating junction temperature	Tjop	ı	-20 to +125	ç	
6	Storage temperature	Tstg	-	-55 to +150	ç	
7	Power dissipation	Pw	•	1.0	W	WQFN48 Ta=70°C

3. Electrical Characteristics

3.1 DC Characteristics

	Table 2 DC Characteristics Ta=25°C VDC=12V VDD=5V												
Na	ltomo	Curahal		Spec		I lm:4	Took conditions						
No.	Items	Symbol	Min	Тур	Max	Unit	Test conditions						
1	Small signal switch on	RONS	_	18	26	Ω	ISIG=5mA						
'	resistance	KONO	I	18	26	\$2	ISIG=200mA						
2	Small signal switch on resistance matching	ΔRONS	l	5	20	%	ISIG=5mA						
3	Large signal switch on resistance	RONL	l	16	_	Ω	ISIG=1A						
4	Value of output bleed resistance	RINT	20	35	50	kΩ	Output switch to RGND IRINT=0.5mA						
5	Switch off leakage	ISOL	_	1	10	μΑ	VSIG=100V						
	per switch	ISOL	-	1(3)	3(7)	mA	VSIG=-100V, 32911 is Enclosed in parenthesis						
6	Switch cut off current	ISCC	_	1	10	μΑ	VSIG=100V or -100V						
7	DC offset switch (off)	DCOFF	-	10	100	mV	100Kohm load (32910FN) No load (32911FN)						
8	DC offset switch (on)	DCON	_	10	100	mV	100Kohm load (32910FN) No load (32911FN)						
9	VDC average current	IDC	ı	_	3	mA	fsw=50kHz, No load						
10	VDC quiescent	IDCQ1	-	10	50	μA	All SWs off						
10	current	IDCQ2	_	10	50	μA	All SWs on, ISIG=5mA						
11	VDC peak current	IDSC	-	_	7	mA	All SWs on, no load, Vsig = -100V						
12	VDD average current	IDD	-	_	3.0	mA	fCLK=5MHz,VDD=5.0V						
13	VDD quiescent current	IDDQ	_	_	10	μA							
14	Data out source current	ISOR	0.45	0.70	_	mA	VOUT=VDD-0.7V						
15	Data out sink current	ISINK	0.45	0.70	_	mA	VOUT=0.7V						

3.2 AC Characteristics

Table 3 AC Characteristics Ta=25°C VDC=12V VDD=5V Spec Unit Test conditions No. Items Symbol Max Min Тур tON VSIG=100V, RL= $10k\Omega$ 1 SW Turn on time 3.0 μS 2 SW Turn off time tOFF 3.0 $VSIG{=}100V,\ RL{=}10k\Omega$ μS 50% duty cycle, fData=fCLK/2 30 MHz VDD= 5.0V 3 Clock frequency **fCLK** 50% duty cycle, fData=fCLK/2 20 MHz VDD=3.3V Clock delay time to DOUT terminal, VDD=3.3V tDO 48 ns data out 33 ns DOUT terminal, VDD=5.0V

	Table 4 AC Chara	Ta=25°C VDC=12V VDD=5V								
Nia	lto-ma	Cumhal		Spec		l lmis	Condition			
No.	Items	Symbol	Min	Тур	Max	Unit				
1	Off capacitance SW to GND	CSG (off)	-	15	_	pF	0V, 1MHz			
2	On Capacitance SW to GND	CSG (on)	ı	25	ı	pF	0V, 1MHz			
3	SW off inclution	КО	-28	-32	1	dB	fsig=5MHz, 1kΩ//15pF load			
3	SW off isolation	KO	-50	-54	_	dB	fsig=5MHz, 50Ω load			
4	SW Crosstalk	KCR	-50	-54	1	dB	fsig=5MHz, 50Ω load			
_		+VSPK		_	40		DI 500			
5	Output voltage spike	-VSPK	-20	_	_	mV	RL=50Ω			

4. Recommended Operating Conditions

Please operate in use within the limit of recommended operating conditions detailed in Table 5.

Table 5 Recommended Operating Conditions

No	Items	Symbol	Recommended Value	Condition
1	Logic power supply voltage	VDD	3.0V to 5.5V	
2	VDC voltage supply	VDC	10V to 15V	
3	High-level input voltage	VIH	0.9VDD to VDD	
4	Low-level input voltage	VIL	0V to 0.1VDD	
5	Analog signal voltage peak to peak	VSIG	-100V to 100V	
	Analog signal fragues as	fair	More than 100KHz	VSIG > 10Vp-p
6	Analog signal frequency	fsig	Not limited	VSIG ≤ 10Vp-p
7	Operating free air-temperature	Та	0°C to 70°C	
8	Switching frequency	fsw	50kHz max, Duty Cycle=50%	
9	Set up time for LE	TSD	Min.60ns	
10	Pulse width of LE	TWLE	Min.40ns	
11	Time width of CL	TWCL	Min.40ns	
12	Set up time DATA to Clock	TSU	Min.10ns	
13	Hold time DATA from Clock	Th	Min.10ns	
14	Maximum VSIG Slew Rate	dV/dt	Max.30V/ns	

Attention;

- 1) GND terminal must be connected during power-up and power-down.
- 2) It is indispensable overshoot/undershoot voltage of power supplies(VDD, VDC) do NOT exceed maximum rated voltage in the event of power-up and power-down.

5. Test Circuit

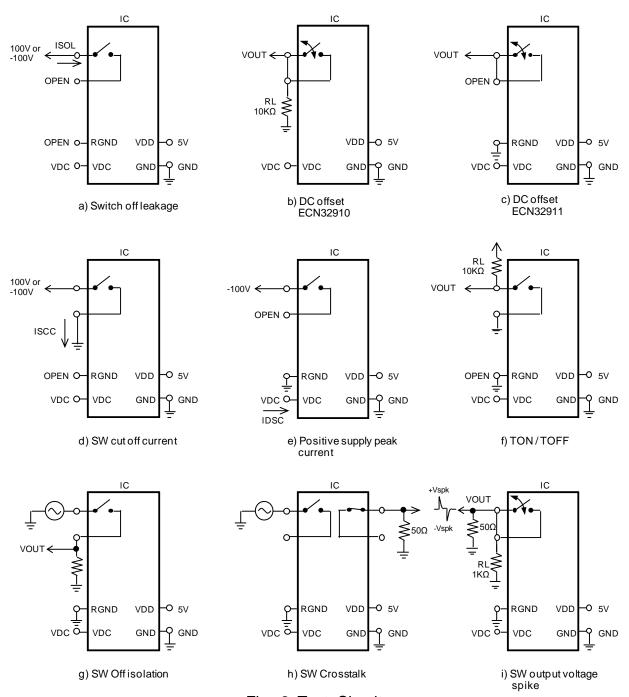


Fig. 2 Test Circuit

6. Timing Waveforms

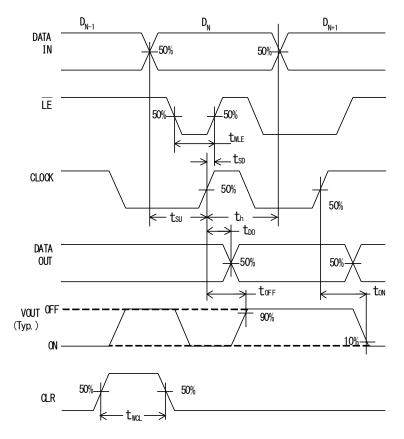


Fig. 3 Timing Waveforms

<u>Note</u>

- 1. Serial data is clocked in on the rising edge of CLK.
- 2. The switches go to a state retaining their present condition on the rising edge of LE.

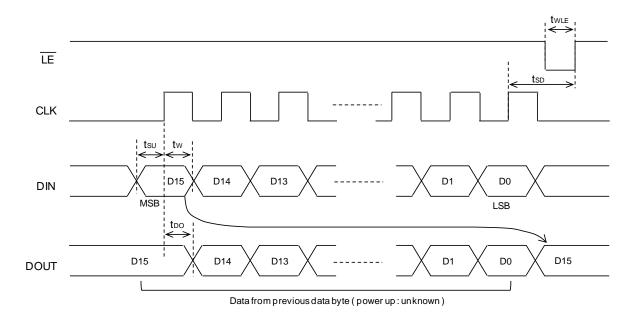


Fig. 4 LATCH ENABLE Timing waveform

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7. Truth Table

Table 6 Truth table

	Table 0 Truth table																
D0	D1	D2	D3	D4	D5	D6	D7	LE	CL	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
Н								L	L	ON							
	L							L	L		OFF						
	Н							L	L		ON						
		L						L	L			OFF					
		Н						L	L			ON					
			Г					L	L				OFF				
			Н					L	L				ON				
				L				L	L					OFF			
				Н				L	L					ON			
					L			L	L						OFF		
					Н			L	L						ON		
						L		L	L							OFF	
						Н		L	L							ON	
							Ĺ	L	L								OFF
							Н	L	Ĺ								ON
Χ	Х	Χ	Χ	Х	Χ	Χ	Х	Н	L	HOLD PREVIOUS STATE							
Х	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Х	Н	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

D8	D9	D10	D11	D12	D13	D14	D15	LE	CL	SW8	SW9	SW10	SW11	SW12	SW13	SW14	SW15
L								L	L	OFF							
Н								L	L	ON							
	L							L	L		OFF						
	Н							L	L		ON						
		L						L	L			OFF					
		Н						L	L			ON					
			L					L	L				OFF				
			Н					L	L				ON				
				L				L	L					OFF			
				Н				L	L					ON			
					L			L	L						OFF		
					Н			L	L						ON		
						L		L	L							OFF	
						Н		L	L							ON	
							L	L	L								OFF
							Н	L	L								ON
Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Н	L			HOLD	PREV	IOUS S	TATE		
Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Н	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

X = Don't care

- 1. The 16 Switches operate independently.
- 2. When \overline{LE} is low, the shift register data flows through the latch.
- 3. Shift register clocking has no effect on the switch states if \overline{LE} is high. 4. When switch 15 is ON, DOUT will be high.
- 5. The clear input overrides all other inputs.

8. Pin Configuration

ECN32910FN/32911FN WQFN48 (48Pin WQFN)

Table7. Pin Configuration

Pin	Name	Functions	Note
1	N/C	No connection	*1
2	N/C	No connection	*1
3	SW4B	Analog Switch 4	
4	SW4A	Analog Switch 4	
5	SW3B	Analog Switch 3	
6	SW3A	Analog Switch 3	
7	SW2B	Analog Switch 2	
8	SW2A	Analog Switch 2	
9	SW1B	Analog Switch 1	
10	SW1A	Analog Switch 1	
11	SW0B	Analog Switch 0	
12	SW0A	Analog Switch 0	
13	GND2	Ground	
14	N/C	No connection	*1
15	VDC	VDC voltage supply	
16	N/C	No connection	*1
17	GND	Ground	
18	VDD	Logic Supply Voltage	
19	DIN	Serial Data Input	
20	CLK	Serial Clock Input	
21	LE	Latch-Enable Input	
22	CLR	Latch-Clear Input	
23	DOUT	Serial Data Output	
24	RGND(N/C)	Ground(ECN32911FN) / No connection(ECN32910FN)	*2
25	SW15B	Analog Switch 15	
26	SW15A	Analog Switch 15	
27	SW14B	Analog Switch 14	
28	SW14A	Analog Switch 14	
29	SW13B	Analog Switch 13	
30	SW13A	Analog Switch 13	
31	SW12B	Analog Switch 12	
32	SW12A	Analog Switch 12	
33	SW11B	Analog Switch 11	
34	SW11A	Analog Switch 11	
35	N/C	No connection	*1
36	N/C	No connection	*1
37	SW10B	Analog Switch 10	
38	SW10A	Analog Switch 10	
39	SW9B	Analog Switch 9	
40	SW9A	Analog Switch 9	
41	SW8B	Analog Switch 8	
42	SW8A	Analog Switch 8	
43	SW7B	Analog Switch 7	
44	SW7A	Analog Switch 7	
45	SW6B	Analog Switch 6	
46	SW6A	Analog Switch 6	
47	SW5B	Analog Switch 5	
48 Note 1	SW5A	Analog Switch 5	

Note 1. NOT connected on chip internal.

2. RGND terminal connects to bleed resistors on chip internal.(ECN32911FN only).

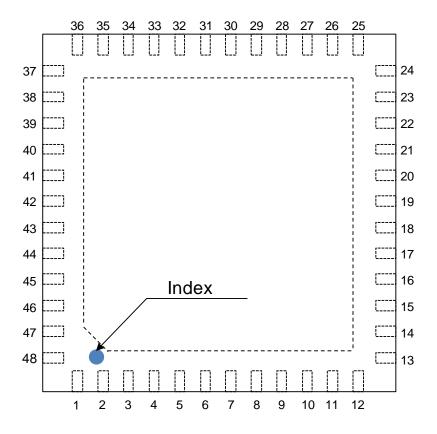


Fig.8 Pin Configuration (Top view)

9. Package Outline

Units: mm

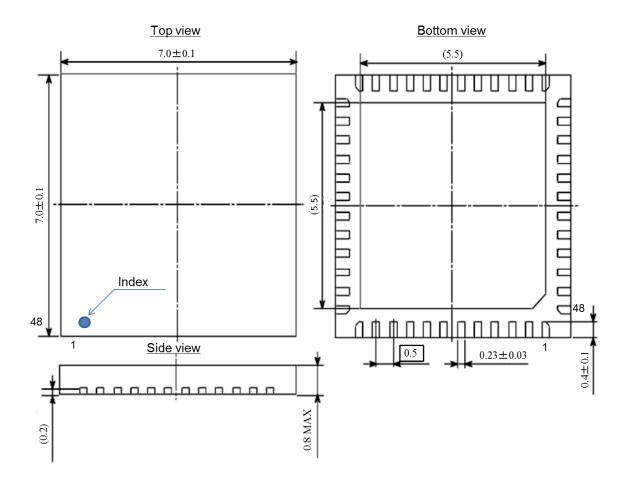


Fig. 9 Package Outline

Note) A tab of the back of a QFN package is connected GND pin with electrically. When IC is mounted on PCB board, please connect it to GND layer.

10. Footprint Pattern

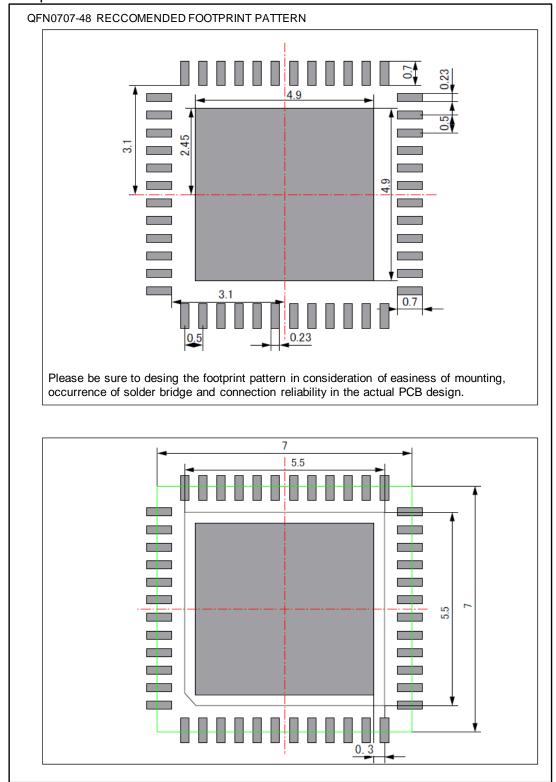


Fig. 10 Foot Pattern Design example

11. Marking spec

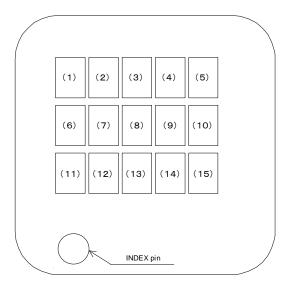


Fig. 11 Marking

Lot numbering rule

1) Mark No. (1): Year code (Least significant digit of Assembled year (A.D.))

2) Mark No. (2): Month code (Refer to following table.)

-					(
	Month	1	2	3	4	5	6	7	8	9	10	11	12		
	Month code	Α	В	С	D	Е	K	L	М	Ν	Х	Υ	Z		

- 3) Mark No. (3) to (5): Quality Control number
- 4) Mark No. (6) to (15): Parts name "ECN32910FN" or "ECN32911FN"
- 5) Mark Method: Laser Mark

12. Packing Form

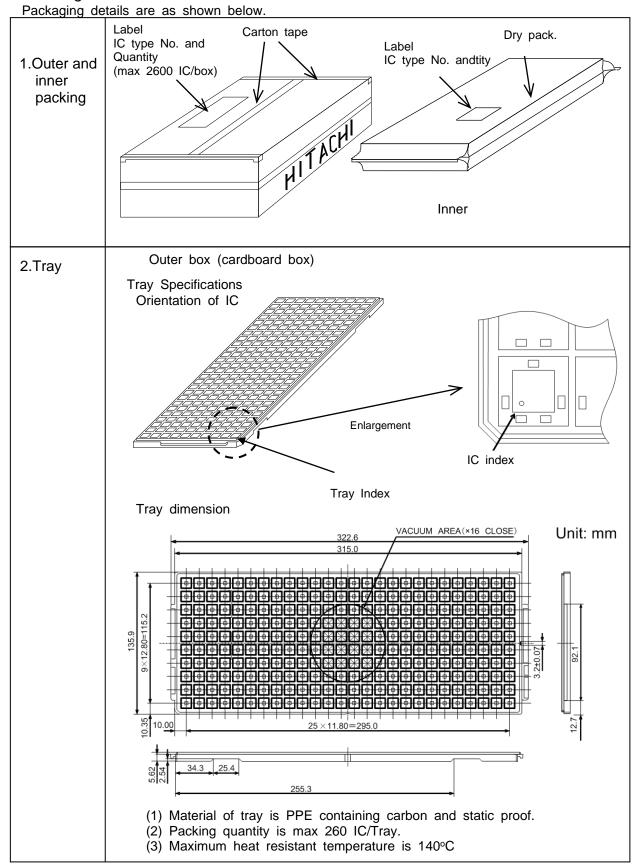


Fig. 12 Packing Form

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13. Inspection

Hundred percent inspections shall be conducted on electric characteristics.

14. Precautions for use

14.1 Countermeasures against Electrostatic Discharge (ESD)

- (a) Customers need to take precautions to protect ICs from electrostatic discharge (ESD). The material of the container or any other device used to carry ICs should be free from ESD, which can be caused by vibration during transportation. Use of electrically conductive containers is recommended as an effective countermeasure.
- (b) Everything that touches ICs, such as the work platform, machine, measuring equipment, and test equipment, should be grounded.
- (c) Workers should be high-impedance grounded (100k Ω to 1M Ω) while working with ICs, to avoid damaging the ICs by ESD.
- (d) Friction with other materials, such as high polymers, should be avoided.
- (e) When carrying a PCB with a mounted IC, ensure that the electric potential is maintained at a constant level using the short-circuit terminals and that there is no vibration or friction.
- (f) The humidity at an assembly line where ICs are mounted on circuit boards should be kept around 45 to 75 percent using humidifiers or such. If the humidity cannot be controlled effectively, using ionized air blowers (ionizers) is effective.

14.2 Maximum ratings

Regardless of changes in external conditions during use IC (the product of Hitachi Power Semiconductor Device, hereinafter called "HPSD's IC"), the "maximum ratings" described in this document should never be exceeded when designing electronic circuits that employ HPSD's IC. If maximum ratings are exceeded, HPSD's IC may be damaged or destroyed. In no event shall Hitachi Power Semiconductor Device (hereinafter called "HPSD") be liable for any failure in HPSD's IC or any secondary damage resulting from use at a value exceeding the maximum ratings.

14.3 Derating Design

Continuous high-load operation (high temperatures, high voltages, large currents) should be avoided and derating design should be applied, even within the ranges of the maximum ratings, to ensure reliability.

14.4 Safe Design

The HPSD's IC may fail due to accidents or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy and measures to prevent misuse, in order to avoid extensive damage in the event of a failure.

14.5 Application

If HPSD's IC is applied to the following uses where high reliability is required, obtain the document of permission from HPSD in advance.

- Automobile, Train, Vessel, etc.

Do not apply HPSD's IC to the following uses where extremely high reliability is required.

· Nuclear power control system, Aerospace instrument, Life-support-related medical equipment, etc.

14.6 Soldering

Lead-free solder is used for coating pins and the tab of this IC.

Refer to "Precautions for Use of High Voltage Monolithic Ics" for soldering conditions.

14.7 Others

See "Instructions for Use of Hitachi High-Voltage Monolithic ICs" for other precautions and instructions on how to deal with these kinds of products.



15. Usage

- (1) HPSD warrants that the HPSD products have the specified performance according to the respective specifications at the time of its sale. Testing and other quality control techniques of the HPSD products by HPSD are utilized to the extent HPSD needs to meet the specifications described in this document. Not every device of the HPSD products is specifically tested on all parameters, except those mandated by relevant laws and/or regulations.
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◆Appendix-Supplementary Data

Please read below contents before using this product.

Function Description

1. Bleed resistor

ECN32911FN feature integrated $35k\Omega$ bleed resistor to discharge capacitive Loads such as piezoelectric transducers. Each analog switch terminal is connected RGND with a bleed resistor.

2. Power supply sequence

ECN32910FN/32911FN doesn't require the power up/down special sequence of the VDC and VDD power supplies.

However, shift register and latch are unsettled just after power-up.

Therefore, it's necessary to set the data of shift register after power-up.

(Please refer to the truth table. : Table.6)

Analog signal frequency

If analog signal peak-to-peak voltage is more than 10Vp-p, the minimum analog signal frequency must be more than 100KHz.

If analog signal peak-to-peak voltage is less than 10Vp-p, the minimum analog signal frequency is not limited.

Storage Conditions

(1) Before opening the moisture prevention bag (aluminum laminate bag)

Temperature: 5 to 35°C Humidity: 85%RH or lower Period: less than 1 year

(2) After opening the moisture prevention bag (aluminum laminate bag)

Temperature: 5°C to 30°C Humidity: 60%RH or lower

Period: less than 1 week (from opening the bag to reflow soldering)

(3) Temporal storage after opening the moisture prevention bag

When ICs are stored temporarily after opening the bag they should be returned into the bag with desiccant within 10 minutes. Then, the open side of the bag should be folded under twice, and closed with adhesive tape. And it should be kept in the following conditions.

Temperature: 5°C to 35°C Humidity: 85%RH or lower Period: less than 1 month

*If it expects to exceed "Period" as stated in (1) to (3), we recommend storing devices in dry cabinet. (25° C +/- 5° C, Less than 30%RH condition)

(4) Baking

When it exceeds "Period" as stated in (1) to (3), please bake devices under the following conditions.

Temperature: 125 +/-5°C Baking time: 16 to 24h

*If devices are stored in dry cabinet, baking is not needed even if storage "Period" exceeds.

Precautions for Safe Use and Notices

If semiconductor devices are handled in an inappropriate manner, failures may result. For this reason, be sure to read the latest version of "Instructions for Use of Hitachi High-Voltage Monolithic ICs" before use.



This mark indicates an item requiring caution.



CAUTION

This mark indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury and damage to property.



CAUTION

- (1) Regardless of changes in external conditions during use of semiconductor devices, the "maximum ratings" and "safe operating area(SOA)" should never be exceeded when designing electronic circuits that employ semiconductor devices.
- (2) Semiconductor devices may fail due to accidents or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy and measures to prevent misuse, in order to avoid extensive damage in the event of a failure.
- (3) If semiconductor devices are applied to uses where high reliability is required, obtain the document of permission from HPSD in advance (Automobile, Train, Vessel, etc.). Do not apply semiconductor devices to uses where extremely high reliability is required (Nuclear power control system, Aerospace instrument, Life-support-related medical equipment, etc.). (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

NOTICES

- 1. This Data Sheet contains the specifications, characteristics, etc. concerning power semiconductor products (hereinafter called "products").
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- 7. In no event shall HPSD be liable for any failure in HPSD products or any secondary damage resulting from use at a value exceeding the maximum ratings.

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