

16-channel High Voltage analog switch IC

ECN3297TF Product Specification

1. General Description

1.1 General

ECN3297 is 16-channel High Voltage analog switching IC with bleed resistors on which latch-up free is realized by dielectric isolation technology.

High voltage and low on-resistance MOS switches are used as output devices controlled by a 3.3V or 5.0V signal. The ECN3297 is most suited to ultrasound imaging applications.

1.2 Functions and Features

- * High voltage and low on-resistance MOS switches integrated.
- * 16bit shift register integrated.
- * Integrated bleed resistors.
- * Integrated clamping diodes for overvoltage protection positive overshoot.
- * Switch on-resistance: 19 Ω typ. (VPP=100V,VNN=-100V,ISIG=5mA, 25°C)
- * Switch breakdown voltage: 220V
- * Power up/down sequence of power supply is free.
- * 48-pin LQFP Package. (RoHS compliant)

1.3 Block diagram

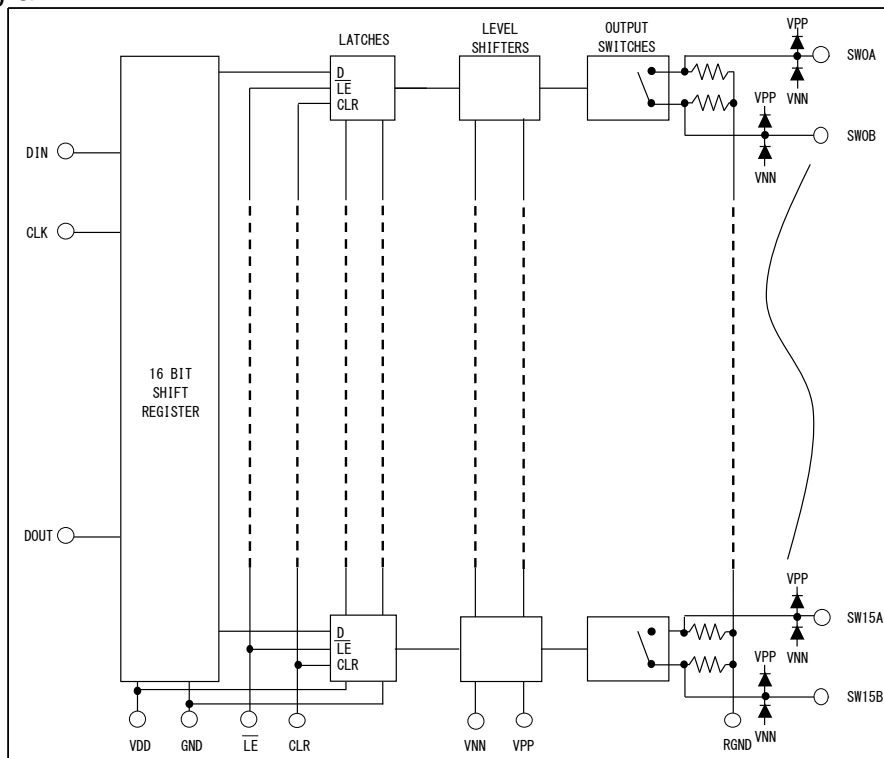


Fig. 1.3.1 Block diagram

2. Specifications

2.1 Absolute Maximum Ratings

Table 2.1.1 Absolute Maximum Ratings

| No. | Items | Symbol | Terminal | Values | Unit | Note |
|-----|----------------------------------|--------|---------------------|-----------------|------|---------|
| 1 | Logic power supply voltage | VDD | VDD | -0.5 to +7.0 | V | Ta=25°C |
| 2 | VPP-VNN supply voltage | - | VPP, VNN | 220 | V | Ta=25°C |
| 3 | VPP Positive high voltage supply | VPP | VPP | -0.5 to 200 | V | Ta=25°C |
| 4 | VNN negative high voltage supply | VNN | VNN | -200 to +0.5 | V | Ta=25°C |
| 5 | Logic input voltages | - | DIN, CLK, CL, LE | -0.5 to VDD+0.3 | V | Ta=25°C |
| 6 | Analog signal range | - | SW0 to SW15 | VNN to VPP | V | Ta=25°C |
| 7 | Operating junction temperature | Tjop | - | -20 to +125 | °C | |
| 8 | Storage temperature | Tstg | - | -55 to +150 | °C | |
| 9 | Power dissipation | Pw | - | 1.0 | W | Ta=70°C |

2.2 Electrical Characteristics

2.2.1 DC Characteristics

Table 2.2.1 DC Characteristics

Ta=25°C VDD=5.0V

| No. | Items | Symbol | Spec | | | Unit | Test conditions | |
|-----|--|--------|------|------|-----|------|---------------------------------------|------------------------|
| | | | Min | Typ | Max | | | |
| 1 | Small signal switch on resistance | RONS | - | 24 | 38 | Ω | ISIG=5mA | VPP=40V, VNN=-160V |
| | | | - | 17 | 27 | | ISIG=200mA | |
| | | | - | 19 | 27 | | ISIG=5mA | VPP=100V, VNN=-100V |
| | | | - | 15 | 24 | | ISIG=200mA | |
| | | | - | 19 | 25 | | ISIG=5mA | VPP=160V, VNN=-40V |
| | | | - | 15 | 25 | | ISIG=200mA | |
| 2 | Small signal switch on resistance matching | ΔRONS | - | 5 | 20 | % | VPP=100V, VNN=-100V ISIG=5mA | |
| 3 | Large signal switch on resistance | RONL | - | 16 | - | Ω | VPP=100V VNN=-100V | ISIG =1A |
| 4 | Value of output bleed resistance | RINT | 20 | 35 | 50 | kΩ | IRINT=0.5mA, Output switch to RGND | |
| 5 | Switch off leakage per switch | ISOL | - | 1.0 | 10 | μA | VSIG=VPP-10V, or VNN+10V | |
| 6 | DC offset switch (off) | DCOFF | - | 10 | 100 | mV | no-load | |
| 7 | DC offset switch (on) | DCON | - | 10 | 100 | mV | no-load | |
| 8 | Positive HV supply current | IPPQ1 | - | 10 | 50 | μA | All SWs off | |
| 9 | Negative HV supply current | INNQ1 | - | -10 | -50 | μA | All SWs off | |
| 10 | Positive HV supply current | IPPQ2 | - | 10 | 50 | μA | All SWs on, ISIG=5mA | |
| 11 | Negative HV supply current | INNQ2 | - | -10 | -50 | μA | All SWs on, ISIG=5mA | |
| 12 | IPP Supply current | IPP | - | - | 7.0 | mA | VPP=40V VNN=-160V | fSW=50kHz no-load |
| | | | - | - | 7.0 | | VPP=100V VNN=-100V | |
| | | | - | - | 8.0 | | VPP=160V VNN=-40V | |
| 13 | INN Supply current | INN | - | - | 7.0 | mA | VPP=40V VNN=-160V | fSW=50kHz no-load |
| | | | - | - | 7.0 | | VPP=100V VNN=-100V | |
| | | | - | - | 8.0 | | VPP=160V VNN=-40V | |
| 14 | Logic supply average current | IDD | - | - | 4.0 | mA | fCLK=5MHz | |
| 15 | Logic supply quiescent current | IDDQ | - | - | 10 | μA | | |
| 16 | Data out source current | ISOR | 0.45 | 0.70 | - | mA | Vdout=VDD-0.7V | |
| 17 | Data out sink current | ISINK | 0.45 | 0.70 | - | mA | Vdout=0.7V | |

2.2.2 AC Characteristics

Table 2.2.2 AC Characteristics Ta=25°C VDD=5.0V

| No. | Items | Symbol | Spec | | | Unit | Test conditions |
|-----|------------------------------|--------|------|-----|------|------|--|
| | | | Min | Typ | Max | | |
| 1 | SW Turn on time | tON | - | - | 5.0 | μs | VSIG=VPP-10V, RL=10kΩ |
| 2 | SW Turn off time | tOFF | - | - | 5.0 | μs | VSIG=VPP-10V, RL=10kΩ |
| 3 | Clock frequency | fCLK | - | - | 30 | MHz | 50% duty cycle, fDIN=fCLK/2 VDD= 5.0V |
| | | | - | - | 20 | MHz | 50% duty cycle, fDIN=fCLK/2 VDD=3.3V |
| 4 | Clock delay time to data out | tDO | 16 | - | 55 | ns | DOUT terminal, VDD=3.3V |
| | | | 12 | - | 42 | ns | DOUT terminal, VDD=5.0V |
| 5 | Output voltage spike | +VSPK | - | - | 150 | mV | VPP=40V, VNN=-160V, RL=50Ω |
| | | -VSPK | - | - | -150 | | |
| | | +VSPK | - | - | 150 | | VPP=100V, VNN=-100V, RL=50Ω |
| | | -VSPK | - | - | -150 | | |
| | | +VSPK | - | - | 150 | | VPP=160V, VNN=-40V, RL=50Ω |
| | | -VSPK | - | - | -150 | | |

2.2.3 AC Characteristics (for reference purpose only)

These items are not tested when shipped.

Table 2.2.3 AC Characteristics (for reference purpose only) Ta=25°C VDD=5.0V

| No. | Items | Symbol | Spec | | | Unit | Condition |
|-----|---------------------------|-----------|------|-----|-----|------|-------------------------------------|
| | | | Min | Typ | Max | | |
| 1 | Off capacitance SW to GND | CSG (off) | - | 6 | - | pF | Measurement signal (DC 0V, AC 1MHz) |
| 2 | On Capacitance SW to GND | CSG (on) | - | 15 | - | pF | Measurement signal (DC 0V, AC 1MHz) |
| 3 | SW off isolation | KO | -30 | -33 | - | dB | f=5MHz, RL=1kΩ//15pF |
| | | | -54 | -60 | - | dB | f=5MHz, RL=50Ω |
| 4 | SW crosstalk | KCR | -54 | -60 | - | dB | f=5MHz, RL=50Ω |

3. Recommended Operating Conditions

Please operate in use within the limit of recommended operating conditions detailed in Table 3.1.

Table 3.1 Recommended Operating Conditions

| No | Items | Symbol | Recommended Value | Unit | Condition |
|----|------------------------------------|--------|-------------------|-------|----------------|
| 1 | Logic power supply voltage | VDD | 3.0 to 5.5 | V | |
| 2 | Positive high voltage supply | VPP | 40 to 160 | V | |
| 3 | Negative high voltage supply | VNN | -160 to 0 | V | |
| 4 | VPP-VNN supply voltage | - | 40 to 200 | V | |
| 5 | High-level input voltage | VIH | 0.9VDD to VDD | V | |
| 6 | Low-level input voltage | VIL | 0 to 0.1VDD | V | |
| 7 | Analog signal voltage peak to peak | VSIG | VNN to VPP | V | |
| 8 | Operating free air-temperature | Ta | 0 to 70 | °C | |
| 9 | Switching frequency | fSW | 50 max | kHz | Duty Cycle=50% |
| 10 | Set up time for \overline{LE} | tSD | Min.60 | ns | |
| 11 | Pulse width of \overline{LE} | tWLE | Min.40 | ns | |
| 12 | Time width of CL | tWCL | Min.40 | ns | |
| 13 | Set up time DATA to Clock | tSU | Min.10 | ns | |
| 14 | Hold time DATA from Clock | th | Min.10 | ns | |
| 15 | Maximum VSIG Slew Rate | dV/dt | Max.30 | V/ ns | |

Attention ;

- 1) Power up/down sequence of power supply is arbitrary except GND terminal of IC must be powered-up first and powered-down last.
- 2) It is indispensable to make there are not to exceed a maximum rated voltage by the occurrence of the excessive voltage in case of power-on and power-off of the power supply.

4. Test Circuit

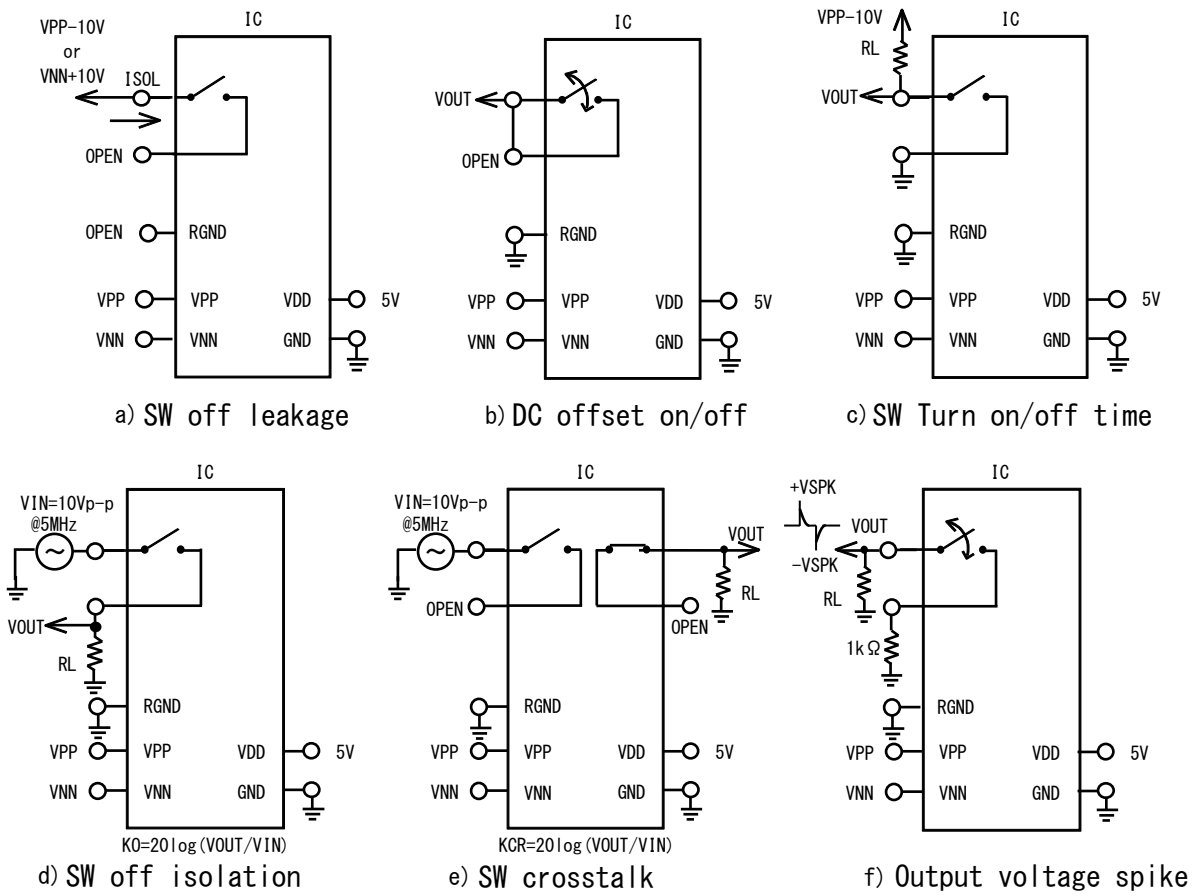


Fig. 4.1 Test Circuit

5. Timing Waveforms

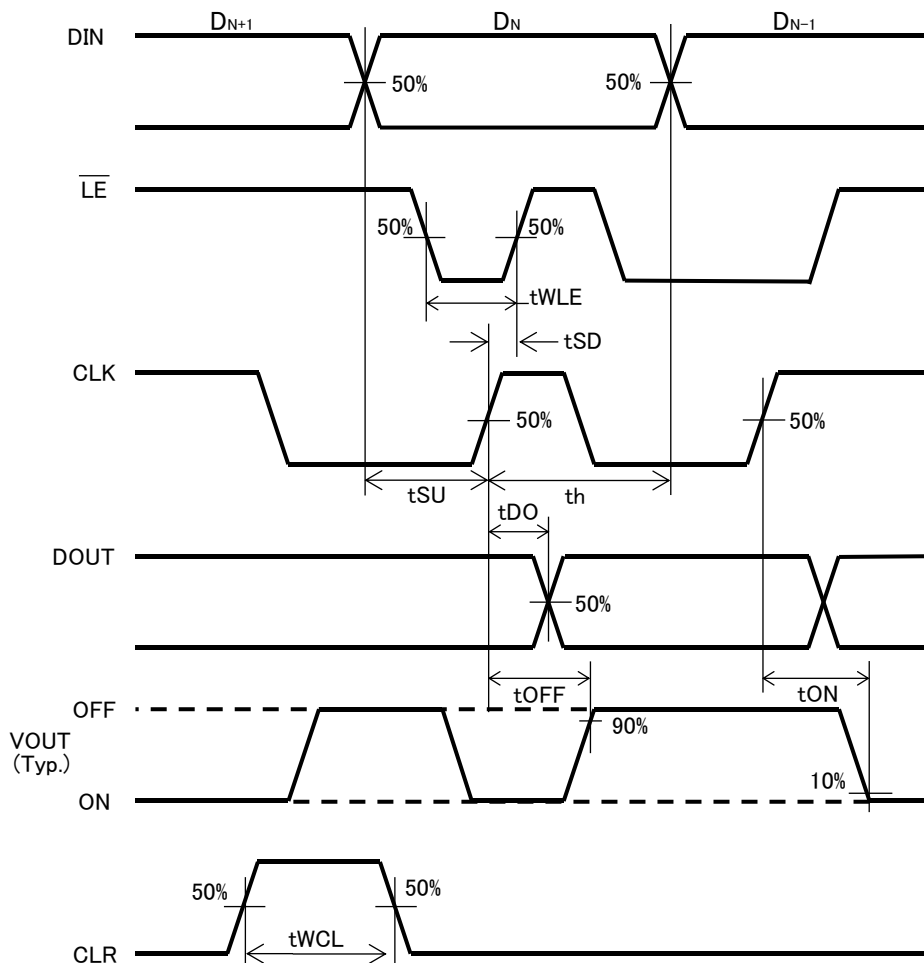


Fig. 5.1 Timing Waveforms

Note

1. Serial data is clocked in on the rising edge of CLK.
2. The switches go to a state retaining their present condition on the rising edge of LE.

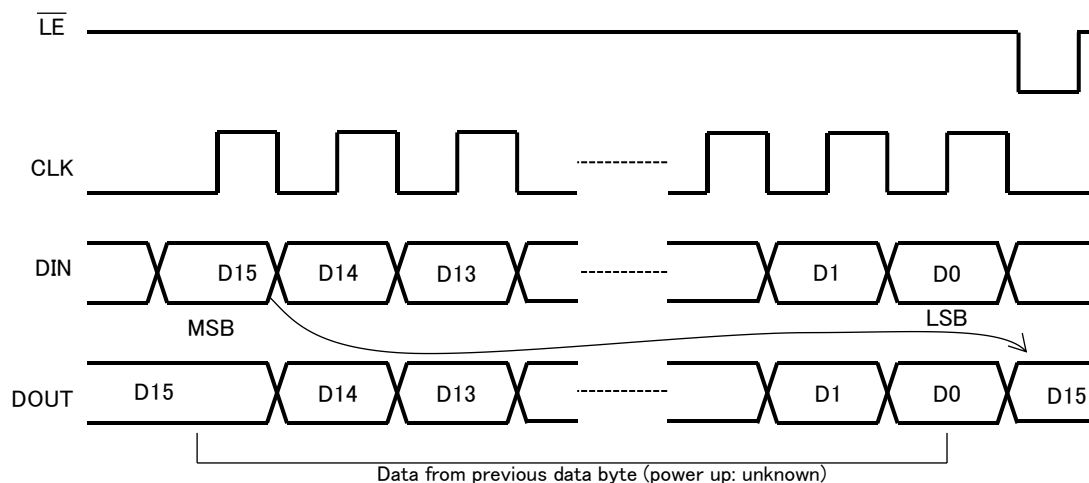


Fig. 5.2 LATCH ENABLE Timing waveforms

6. Truth Table

Table 6.1 Truth table

| D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | \overline{LE} | CLR | SW0 | SW1 | SW2 | SW3 | SW4 | SW5 | SW6 | SW7 |
|----|----|----|----|----|----|----|----|-----------------|-----|---------------------|-----|-----|-----|-----|-----|-----|-----|
| L | | | | | | | | L | L | OFF | | | | | | | |
| H | | | | | | | | L | L | ON | | | | | | | |
| | L | | | | | | | L | L | | OFF | | | | | | |
| | H | | | | | | | L | L | | ON | | | | | | |
| | | L | | | | | | L | L | | | OFF | | | | | |
| | | H | | | | | | L | L | | | ON | | | | | |
| | | | L | | | | | L | L | | | | OFF | | | | |
| | | | H | | | | | L | L | | | | ON | | | | |
| | | | | L | | | | L | L | | | | | OFF | | | |
| | | | | H | | | | L | L | | | | | ON | | | |
| | | | | | L | | | L | L | | | | | | OFF | | |
| | | | | | H | | | L | L | | | | | | ON | | |
| | | | | | | L | | L | L | | | | | | | OFF | |
| | | | | | | H | | L | L | | | | | | | ON | |
| | | | | | | | L | L | L | | | | | | | | OFF |
| | | | | | | | H | L | L | | | | | | | | ON |
| X | X | X | X | X | X | X | X | H | L | HOLD PREVIOUS STATE | | | | | | | |
| X | X | X | X | X | X | X | X | X | H | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF |

| D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | \overline{LE} | CLR | SW8 | SW9 | SW10 | SW11 | SW12 | SW13 | SW14 | SW15 |
|----|----|-----|-----|-----|-----|-----|-----|-----------------|-----|---------------------|-----|------|------|------|------|------|------|
| L | | | | | | | | L | L | OFF | | | | | | | |
| H | | | | | | | | L | L | ON | | | | | | | |
| | L | | | | | | | L | L | | OFF | | | | | | |
| | H | | | | | | | L | L | | ON | | | | | | |
| | | L | | | | | | L | L | | | OFF | | | | | |
| | | H | | | | | | L | L | | | ON | | | | | |
| | | | L | | | | | L | L | | | | OFF | | | | |
| | | | H | | | | | L | L | | | | ON | | | | |
| | | | | L | | | | L | L | | | | | OFF | | | |
| | | | | H | | | | L | L | | | | | ON | | | |
| | | | | | L | | | L | L | | | | | | OFF | | |
| | | | | | H | | | L | L | | | | | | ON | | |
| | | | | | | L | | L | L | | | | | | | OFF | |
| | | | | | | H | | L | L | | | | | | | ON | |
| | | | | | | | L | L | L | | | | | | | | OFF |
| | | | | | | | H | L | L | | | | | | | | ON |
| X | X | X | X | X | X | X | X | H | L | HOLD PREVIOUS STATE | | | | | | | |
| X | X | X | X | X | X | X | X | X | H | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF |

X = Don't care

Note

1. The 16 Switches operate independently.
2. When \overline{LE} is low, the shift register data flows through the latch.
3. Shift register clocking has no effect on the switch states if \overline{LE} is high.
4. When switch 15 is ON, DOUT is high.
5. The clear input overrides all other inputs.

7. Pin Function

ECN3297TF LQFP48 (48Pin LQFP)

Table 7.1. Pin Function

| Pin | Name | Functions | Note |
|-----|-------|------------------------------------|------|
| 1 | N/C | No connection | *1 |
| 2 | N/C | No connection | *1 |
| 3 | SW4B | Analog Switch 4 | |
| 4 | SW4A | Analog Switch 4 | |
| 5 | SW3B | Analog Switch 3 | |
| 6 | SW3A | Analog Switch 3 | |
| 7 | SW2B | Analog Switch 2 | |
| 8 | SW2A | Analog Switch 2 | |
| 9 | SW1B | Analog Switch 1 | |
| 10 | SW1A | Analog Switch 1 | |
| 11 | SW0B | Analog Switch 0 | |
| 12 | SW0A | Analog Switch 0 | |
| 13 | VNN | Negative High Voltage Supply | *2 |
| 14 | N/C | No connection | *1 |
| 15 | VPP | Positive High Voltage Supply | *2 |
| 16 | N/C | No connection | *1 |
| 17 | GND | Ground | |
| 18 | VDD | Logic Supply Voltage | |
| 19 | DIN | Serial Data Input | |
| 20 | CLK | Serial Clock Input | |
| 21 | LE | Latch-Enable Input | |
| 22 | CLR | Latch-Clear Input | |
| 23 | DOUT | Serial Data Output | |
| 24 | RGND | Ground. Connect to Bleed Resister. | *3 |
| 25 | SW15B | Analog Switch 15 | |
| 26 | SW15A | Analog Switch 15 | |
| 27 | SW14B | Analog Switch 14 | |
| 28 | SW14A | Analog Switch 14 | |
| 29 | SW13B | Analog Switch 13 | |
| 30 | SW13A | Analog Switch 13 | |
| 31 | SW12B | Analog Switch 12 | |
| 32 | SW12A | Analog Switch 12 | |
| 33 | SW11B | Analog Switch 11 | |
| 34 | SW11A | Analog Switch 11 | |
| 35 | N/C | No connection | *1 |
| 36 | N/C | No connection | *1 |
| 37 | SW10B | Analog Switch 10 | |
| 38 | SW10A | Analog Switch 10 | |
| 39 | SW9B | Analog Switch 9 | |
| 40 | SW9A | Analog Switch 9 | |
| 41 | SW8B | Analog Switch 8 | |
| 42 | SW8A | Analog Switch 8 | |
| 43 | SW7B | Analog Switch 7 | |
| 44 | SW7A | Analog Switch 7 | |
| 45 | SW6B | Analog Switch 6 | |
| 46 | SW6A | Analog Switch 6 | |
| 47 | SW5B | Analog Switch 5 | |
| 48 | SW5A | Analog Switch 5 | |

- Note**
1. NOT connected on chip internal.
 2. High voltage supply.
 3. Connected all analog switches with bleed resistor on chip internal.

8. Pin configuration

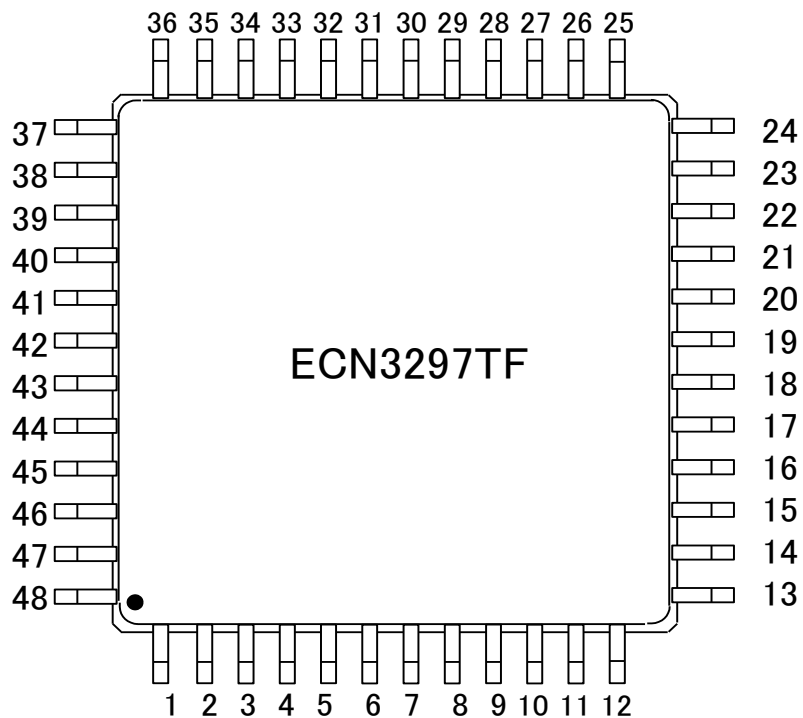


Fig. 8.1 Pin configuration(Top view)

9. Inspection

Hundred percent inspections shall be conducted on electric characteristics.

10. Precautions for use

10.1 Countermeasures against Electrostatic Discharge (ESD)

- (a) Customers need to take precautions to protect ICs from electrostatic discharge (ESD). The material of the container or any other device used to carry ICs should be free from ESD, which can be caused by vibration during transportation. Use of electrically conductive containers is recommended as an effective countermeasure.
- (b) Everything that touches ICs, such as the work platform, machine, measuring equipment, and test equipment, should be grounded.
- (c) Workers should be high-impedance grounded (100kΩ to 1MΩ) while working with ICs, to avoid damaging the ICs by ESD.
- (d) Friction with other materials, such as high polymers, should be avoided.
- (e) When carrying a PCB with a mounted IC, ensure that the electric potential is maintained at a constant level using the short-circuit terminals and that there is no vibration or friction.
- (f) The humidity at an assembly line where ICs are mounted on circuit boards should be kept around 45 to 75 percent using humidifiers or such. If the humidity cannot be controlled effectively, using ionized air blowers (ionizers) is effective.

10.2 Output Short-circuit Protection

This IC (the product of Hitachi Power Semiconductor Device, hereinafter called "HPSD's IC") could break by a short circuit (ex. load short). Therefore, external protection is needed.

10.3 Maximum Ratings

Regardless of changes in external conditions during use of HPSD's IC, the "maximum ratings" described in this document should never be exceeded when designing electronic circuits that employ HPSD's IC. If maximum ratings are exceeded, HPSD's IC may be damaged or destroyed. In no event shall Hitachi Power Semiconductor Device (hereinafter called "HPSD") be liable for any failure in HPSD's IC or any secondary damage resulting from use at a value exceeding the maximum ratings.

10.4 Derating Design

Continuous high-load operation (high temperatures, high voltages, large currents) should be avoided and derating design should be applied, even within the ranges of the maximum ratings, to ensure reliability.

10.5 Safe Design

The HPSD's IC may fail due to accidents or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy and measures to prevent misuse, in order to avoid extensive damage in the event of a failure.

10.6 Application

If HPSD's IC is applied to the following uses where high reliability is required, obtain the document of permission from HPSD in advance.

- Automobile, Train, Vessel, etc.

Do not apply HPSD's IC to the following uses where extremely high reliability is required.

- Nuclear power control system, Aerospace instrument, Life-support-related medical equipment, etc.

10.7 Soldering

Lead-free solder is used for coating pins and the tab of this IC.

Refer to "Precautions for Use of High Voltage Monolithic Ics" for soldering conditions.

10.8 Storage Conditions

- (1) Before opening the moisture prevention bag (aluminum laminate bag)

Temperature: less than 40°C

Humidity: less than 90%RH

Period: less than 12 months

- (2) After opening the moisture prevention bag (aluminum laminate bag)

Temperature: 5°C to 30°C

Humidity: less than 60%RH

Period: less than 168 hours

- ※ When the period of (1) and (2) is likely to expire, store the IC in a drying furnace (10%RH or lower) at ordinary temperature.

- (3) Baking process

When the period of (1) and (2) has expired, the IC should be baked in accordance with the following conditions. (However, when the IC is stored in a drying furnace (10%RH or lower) ordinary temperature, there is no need to bake.) Do not bake the tape and the reel of the taping package because they are not heat resistant. Transfer the IC to a heat resistant container prior to baking.

Temperature: 125°C to 135°C

Period: more than 48 hours

10.9 Others

See "Instructions for Use of Hitachi High-Voltage Monolithic ICs" for other precautions and instructions on how to deal with these kinds of products.

11. Usage

- (1) HPSD warrants that the HPSD products have the specified performance according to the respective specifications at the time of its sale. Testing and other quality control techniques of the HPSD products by HPSD are utilized to the extent HPSD needs to meet the specifications described in this document. Not every device of the HPSD products is specifically tested on all parameters, except those mandated by relevant laws and/or regulations.
- (2) Following any claim regarding the failure of a product to meet the performance described in this document made within one month of product delivery, all the products in relevant lot(s) shall be re-tested and re-delivered. The HPSD products delivered more than one month before such a claim shall not be counted for such response.
- (3) HPSD assumes no obligation nor makes any promise of compensation for any fault which should be found in a customer's goods incorporating the products in the market. If a product failure occurs for reasons obviously attributable to HPSD and a claim is made within six months of product delivery, HPSD shall offer free replacement or payment of compensation. The maximum compensation shall be the amount paid for the products, and HPSD shall not assume responsibility for any other compensation.
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◆Appendix-Supplementary Data

1. Package Outline

Units : mm

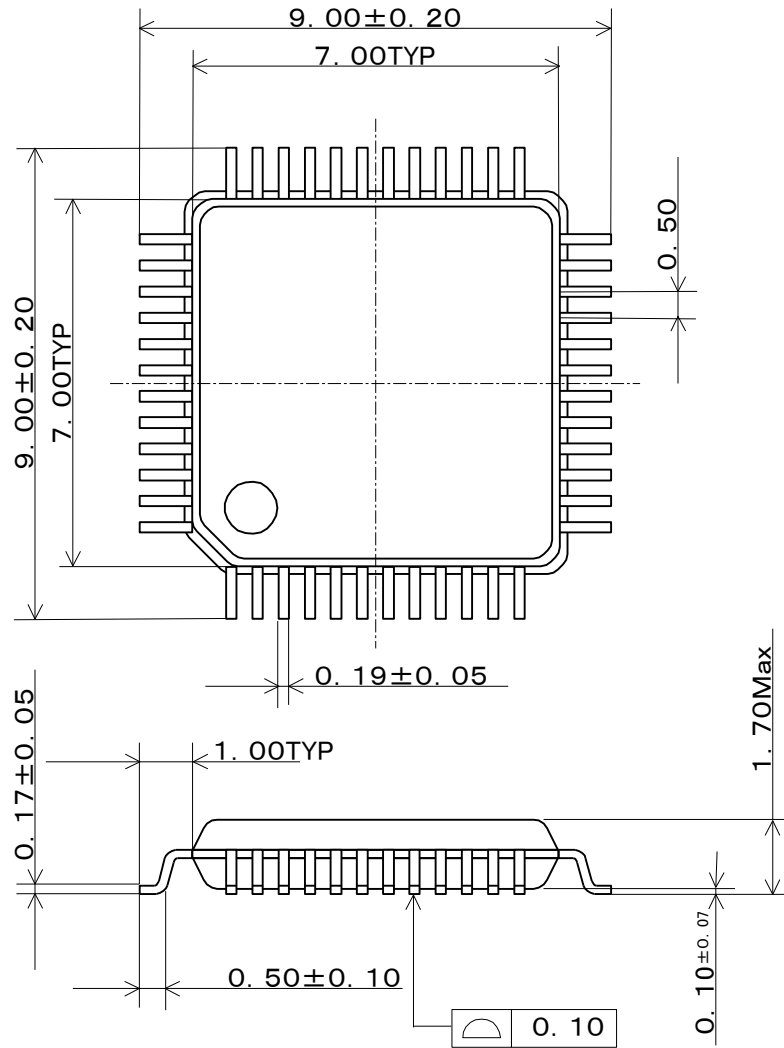


Fig.A Package outline

2. Marking spec

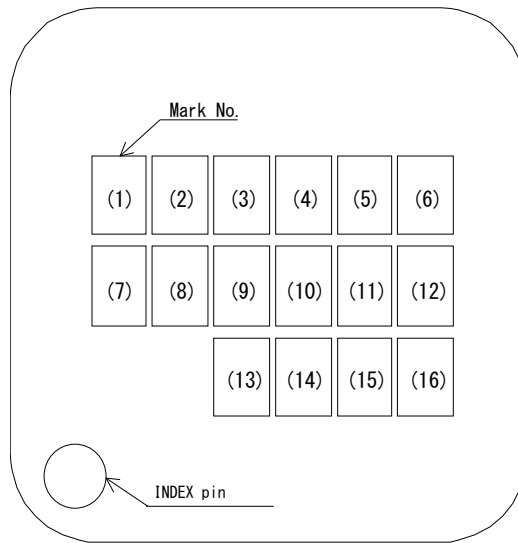


Fig.B Marking

- 1) No.(1) ; Blank
- 2) No.(2)~(6) ; Manufacturing No.
 - No.(2) ; Year code (Least significant digit of Assembled year (A.D.))
 - No.(3) ; Month code (Refer to below.)
 - Jan. ; A, Feb. ; B, Mar. ; C, Apr. ; D,
 - May ; E, June ; K, July ; L, Aug. ; M,
 - Sep. ; N, Oct. ; X, Nov. ; Y, Dec. ; Z
 - No.(4)~(6) ; Serial number
- 3) No.(7) ; Blank
- 4) No.(8)~(16) ; Product name ; ECN3297TF

3. Packing Form

Packaging details are as shown below.

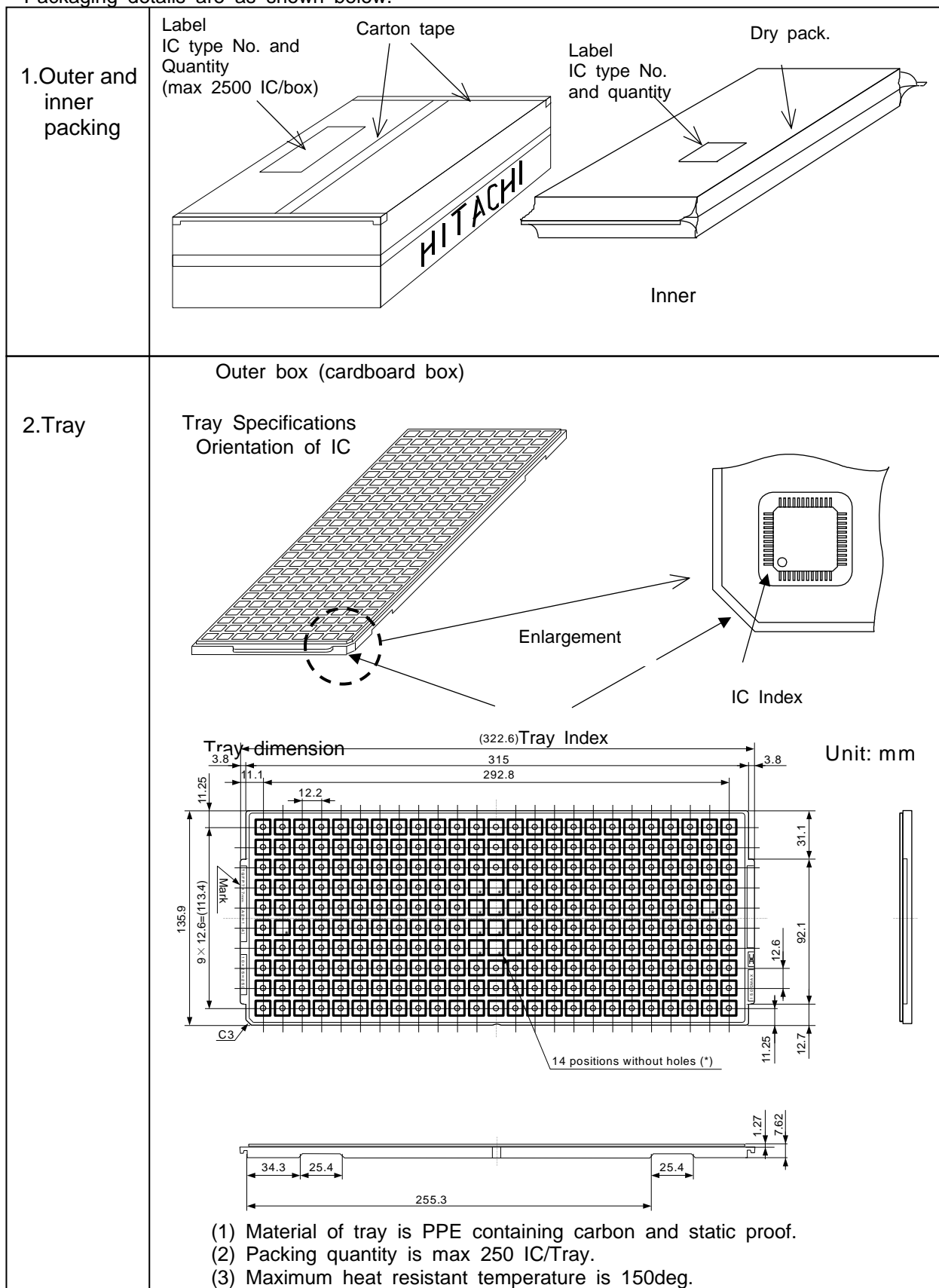


Fig.C IC packing detail

4. Function Description

1. Bleed resistor

ECN3297TF has integrated 35kΩ bleed resistor to discharge capacitive Loads such as piezoelectric transducers. Each analog switch terminal is connected RGND with a bleed resistor.

2. Overvoltage Protection

ECN3297TF feature clamping diodes to protect circuit against the overvoltage exceed VPP or VNN. ALL analog switches connect VPP and VNN terminals with clamping diode.

Normally, switch input voltage must not exceed VNN and VPP, and maximum current flows through the clamping diode should be less than 1A.

3. Power supply sequence free

ECN3297TF doesn't require special sequencing of the VPP, VNN, and VDD supply voltages. However, logic state is unsettled when power-up. After power-up, please refer to the truth table (Page.8 Table.6.1) and set the data of shift register.

Precautions for Safe Use and Notices

If semiconductor devices are handled in an inappropriate manner, failures may result. For this reason, be sure to read the latest version of "Instructions for Use of Hitachi High-Voltage Monolithic ICs" before use.



This mark indicates an item requiring caution.



CAUTION

This mark indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury and damage to property.



CAUTION

- (1) Regardless of changes in external conditions during use of semiconductor devices, the "maximum ratings" and "safe operating area(SOA)" should never be exceeded when designing electronic circuits that employ semiconductor devices.
- (2) Semiconductor devices may fail due to accidents or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy and measures to prevent misuse, in order to avoid extensive damage in the event of a failure.
- (3) If semiconductor devices are applied to uses where high reliability is required, obtain the document of permission from HPSD in advance (Automobile, Train, Vessel, etc.). Do not apply semiconductor devices to uses where extremely high reliability is required (Nuclear power control system, Aerospace instrument, Life-support-related medical equipment, etc.).
(If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

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