3-Phase Gate Driver IC Application Guide

[ R1 ]

Applicable models

<table>
<thead>
<tr>
<th>For ≦ AC115V</th>
<th>ECN30300S</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ECN30301S</td>
</tr>
</tbody>
</table>

Hitachi Power Semiconductor Device, Ltd.
Precautions for Safe Use and Notices

If semiconductor devices are handled in an inappropriate manner, failures may result. For this reason, be sure to read this “Application Guide” before use.

⚠️ This mark indicates an item about which caution is required.

⚠️ CAUTION This mark indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury and damage to property.

CAUTION

1. Regardless of changes in external conditions during use “absolute maximum ratings” should never be exceed in designing electronic circuits that employ semiconductors. In the case of pulse use, Furthermore, “safe operating area (SOA)” precautions should be observed.

2. Semiconductor devices may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure.

3. In cases where extremely high reliability is required (such as in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment), safety should be ensured by using semiconductor devices that feature assured safety or by means of user’s fail-safe precautions or other arrangement. Or consult Hitachi’s sales department staff.

(If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst)

NOTICES

1. This Application Guide contains the specifications, characteristics (in figures and tables), dimensions and handling notes concerning power semiconductor products (hereinafter called “products”) to aid in the selection of suitable products.

2. The specifications and dimensions, etc. stated in this Application Guide are subject to change without prior notice to improve products characteristics. Before ordering, purchasers are advised to contact Hitachi’s sales department for the latest version of this Application Guide and specifications.

3. In no event shall Hitachi be liable for any damage that may result from an accident or any other cause during operation of the user’s units according to this Application Guide. Hitachi assumes to responsibility for any intellectual property claims or any other problems that may result from applications of information, products or circuits described in this Application Guide.

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## Revision History

<table>
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<th>Date</th>
<th>Page</th>
<th>Item No.</th>
<th>Revision</th>
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<td>0</td>
<td>July 10, 2011</td>
<td>—</td>
<td>—</td>
<td>Newly issued</td>
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<td>Sep 4, 2013</td>
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0. Applicable models

<table>
<thead>
<tr>
<th>Commercial AC power</th>
<th>Type</th>
<th>Tachometer output signal frequency (FG)</th>
<th>Product Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>For ≥ AC115V</td>
<td>ECN30300S</td>
<td>(RPM/60)×(P/2)×3 Hz</td>
<td>No.IC-SP-09019</td>
</tr>
<tr>
<td></td>
<td>ECN30301S</td>
<td>(RPM/60)×(P/2)×1 Hz</td>
<td></td>
</tr>
</tbody>
</table>

1. Overview

1.1 Dielectric isolation (DI)

- HITACHI Intelligent Power IC
- A logical device and a power-switching device can be integrated in a single chip.
- No mutual interference occurs, not only between devices but also between device and board.

The Hitachi high-voltage monolithic IC is an intelligent power IC, developed based on a unique dielectric isolation technology (DI). It is structured that there be no latch-up between devices and between device and board, and that an IC can be made so a high-dielectric-strength, large-current output circuit is mixed with a logical circuit. The ICs can be made smaller than conventional discrete boards and hybrid ICs.

- Latch-up-free IC offers wider range of applications.

The Hitachi high-voltage monolithic IC developed with dielectric isolation technology are such that the devices are isolated with SiO₂ layers in between, unlike P-N junction isolation. In consequence, it can remain latched-up free even under high-temperature, large-current, high-noise, and other severe conditions. This technology also enables them to be extremely flexible in circuit designing and thus to meet more customer requirement.

![FIGURE 1.1.1 Dielectric isolation and P-N junction isolation](image-url)
1.2 Gate Driver ICs

Hitachi Gate Driver ICs are monolithic ICs integrating various constituent devices and circuits required for inverter control on a single chip with dielectric isolation technology. They are for driving motors, best suited for controlling small three-phase brushless DC motors. The advantage of downsizing by the use of a single-chip structure can be used to reduce the control board in size, which facilitates the incorporate of such ICs in motors.

![Diagram of Gate Driver IC](image)

**FIGURE 1.2.1 Example of embedded Gate Driver IC**

1.3 Composition of an inverter with Gate Driver IC

An inverter is a device that converts DC currents into AC. It can be used to drive motors for efficient variable-speed control. Figure 1.3.1 shows the basic configuration of an inverter required for that purpose. To drive the three-phase motor with an inverter, six MOSs/IGBTs and free wheel diodes are used as output stages. The IC consists of a MOS/IGBT driving power circuit, level shift circuit, a logic circuit and other components for MOS/IGBT control. Hitachi Gate Driver ICs can directly receive high voltage supplied from rectifying commercial AC power, because they have high dielectric strength. This obviates the need of a step-down circuit, thus inhibiting efficiency cuts induced by voltage conversion.

![Diagram of Inverter with Gate Driver IC](image)

**FIGURE 1.3.1 Basic configuration of an inverter with gate driver IC**
1.4 Motor drive system

Three-phase inverters generally fall into two categories according to the method of commutation of the six output-stage devices: 120-degree energization and 180-degree energization. The method of 120-degree energization is such that the device on the top arm and that on the bottom arm are controlled to set the energization period between phases to 120 degrees, thus transferring the current from phase U to V to W, thus driving the motor. Hitachi Single-chip Gate Driver ICs (VSP-input series) are based on 120-degree energization and receive position signals from Hall elements and VSP signal that constitute speed instructions, thus conducting PWM control by the chopping action of the lower arm. For uses of 180-degree energization, a six-input series are provided where six output stage devices can be controlled by each input signal.

1.5 Block Diagram of Gate Driver ICs

Fig. 1.5.1 shows a block diagram of ECN30300, 30301 these block diagrams are compatible. Its main function is to receive input signals from the three phases of Hall elements of the brushless DC motor, turn on and shut the particular MOSs/IGBTs with the three-phase distribution circuit, and drive the motor. Other components include a charge pump circuit as a power self-supply circuit, a triangular wave oscillator and a comparator-based PWM generation circuit as rpm control circuits, an over current detection circuit which provides a current trip function at motor startup, and an under voltage detection circuit that detects power drops in the drive circuit and turns off the MOSs/IGBTs.
1.6 Comparison with existing products

ECN3030F, ECN3031F are existing products. (ECN3030F Series)

The comparison between these products and new products series ECN30300S is shown in Table 1.6.1.

<table>
<thead>
<tr>
<th>Table 1.6.1 Comparison with existing products</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>No.</strong></td>
</tr>
<tr>
<td>---------</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>3</td>
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<td>22</td>
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<td>23</td>
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<tr>
<td></td>
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<tr>
<td>24</td>
</tr>
<tr>
<td>25</td>
</tr>
</tbody>
</table>

Note1. This table is for reference only. Information is not guaranteed. Please see individual product specification sheets.
FIGURE 1.6.1 Block diagram of ECN3030F
2. Content of product specification

The following items have been described in the product specification.

(1) General
• It describes Type, Application, Structure and Package.

(2) Absolute Maximum Ratings
• It describes direct conditions (electric, thermal use conditions) of leading to IC destruction and so on. And the safety operating range with operating conditions is shown by minimum or maximum value.
• Each item is an independent item. Also, these items show the ratings value of not exceeding any use conditions. The maximum rating and other characteristics are mutually related, and not permitted at the same time.

(3) Electrical Characteristics
• It provides for an electric characteristic item that shows the function of IC, and describes minimum, standard, and maximum.

(4) Function and Operation
• It describes Truth Table, Time Chart, Protection, Function and so on.

(5) Standard applications
• It describes external components to operate IC.

(6) Pin Assignments
• It describes pin assignments and pin names.

(7) Terminal (Pin) Definitions
• It describes Terminal (pin) definitions.

(8) Inspection
• It describes inspection conditions.

(9) Caution
• It describes notes of the static electricity, the maximum rating, handling and so on.

(10) Important Notices
• It describes Productions, Sales, Compensation and so on.

(11) Appendix and Reference data
• It describes Package dimensions, marking and so on.
3. Derating considerations

If a device is used under overload conditions, there is a possibility that reliability will be significantly decreased even if absolute maximum ratings are not exceeded. Determining the derating degree for absolute maximum ratings is an important problem in reliability design. Although derating items to be considered at the system design stage vary slightly depending on the device type, they include electrical stress deratings such as voltage, current, power, load, and environmental stress such as temperature and humidity, and mechanical stress deratings for vibration or shock.

Consideration of derating standards is desirable at the device design stage to ensure reliability. When designing within standards is difficult, other steps become necessary such as selecting a device with higher absolute maximum ratings. Please consult our technical department beforehand. Derating standards that should be considered during reliability design are shown in Table 3.1.

<table>
<thead>
<tr>
<th>Derating factor</th>
<th>IC condition</th>
</tr>
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<tbody>
<tr>
<td>Junction Operating Temp. (Tjop)</td>
<td>Under 110°C</td>
</tr>
<tr>
<td>VS Supply Voltage (VSop)</td>
<td>Under 185V</td>
</tr>
</tbody>
</table>
### 4. Terminal (Pin) definitions

#### Table 4.1.1 Terminal (Pin) definitions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Definition</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>FG</td>
<td>Tachometer output signal. Frequency is (RPM/60)×(P/2)×3 Hz by ECN30300 and (RPM/60)×(P/2)×1 Hz by ECN30301.</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>HUP</td>
<td>Plus Input signal from the Hall element of phase-U</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>HUN</td>
<td>Minus Input signal from the Hall element of phase-U</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>HVP</td>
<td>Plus Input signal from the Hall element of phase-V</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>HVN</td>
<td>Minus Input signal from the Hall element of phase-V</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>HWP</td>
<td>Plus Input signal from the Hall element of phase-W</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>HWN</td>
<td>Minus Input signal from the Hall element of phase-W</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>VSP</td>
<td>Input analog voltage that varies the PWM duty cycle from 0% to 100%</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>CR</td>
<td>Connect resistor &amp; capacitor to generate the PWM clock frequency</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>VTR</td>
<td>Connect resistor to generate the PWM clock frequency</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>RS</td>
<td>Rs voltage input for over current limit operation</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>CB</td>
<td>Internal regulated (VB) power supply output</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>NGU</td>
<td>BOTTOM Arm Gate Drive for Phase-U</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>NGV</td>
<td>BOTTOM Arm Gate Drive for Phase-V</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>NGW</td>
<td>BOTTOM Arm Gate Drive for Phase-W</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>GH</td>
<td>BOTTOM Arm Reference Terminal. Connect RS.</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>GND</td>
<td>Analog ground</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>VCC</td>
<td>Analog/Logic power supply</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>CL</td>
<td>For the Charge Pump circuit</td>
<td>Note1</td>
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<tr>
<td>20</td>
<td>VS</td>
<td>BLDC Motor Power Bus</td>
<td>Note1</td>
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<td>21</td>
<td>C+</td>
<td>For the Charge Pump circuit, power supply for Top Arm drive circuit</td>
<td>Note1</td>
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<td>PGW</td>
<td>TOP Arm Gate Drive for Phase-W</td>
<td>Note1</td>
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<tr>
<td>23</td>
<td>MW</td>
<td>TOP Arm Reference Terminal for Phase-W</td>
<td>Note1</td>
</tr>
<tr>
<td>24</td>
<td>PGV</td>
<td>TOP Arm Gate Drive for Phase-V</td>
<td>Note1</td>
</tr>
<tr>
<td>25</td>
<td>MV</td>
<td>TOP Arm Reference Terminal for Phase-V</td>
<td>Note1</td>
</tr>
<tr>
<td>26</td>
<td>N.C</td>
<td>No Connection</td>
<td>Note2</td>
</tr>
<tr>
<td>27</td>
<td>PGU</td>
<td>TOP Arm Gate Drive for Phase-U</td>
<td>Note1</td>
</tr>
<tr>
<td>28</td>
<td>MU</td>
<td>TOP Arm Reference Terminal for Phase-U</td>
<td>Note1</td>
</tr>
</tbody>
</table>

Note1. This is a high voltage pin. Apply coating or molding treatment to keep the insulation.

Note2. Not connected to the internal IC chip.
### 4.2 Functions of the Pins

#### Table 4.2.1 List of pins and their functions (pins common to all models)

<table>
<thead>
<tr>
<th>No.</th>
<th>Pin</th>
<th>Item</th>
<th>Function and Precaution</th>
<th>Related item</th>
<th>Remark</th>
</tr>
</thead>
</table>
| 1   | VCC   | Control power supply pin                | • Powers the drive circuits for the top and bottom arms, the charge pump circuit, the built-in VB supply circuit, and others.  
• When an external circuit is connected to the CB pin, this pin may be oscillated by the higher load current. If the terminal oscillations, reduce the line impedance by adding the capacitor or decreasing the resistance of line.  
• Determine the capacity of the power supply for VCC allowing a margin by adding the standby current Icc and the current taken out of CB pin. | 5.1 (1) Detection of VCC under voltage  
5.4 Power supply sequence  
8.3 to 8.7 IC destruction by external surge or line noise |                                                          |
| 2   | VS    | High voltage power supply pin           | • Connected to the circuits of the top arm driver and the charge pump.                  | 5.4 Power supply sequence  
8.3 to 8.5 IC destruction by external surge | High voltage pin |
| 3   | CB    | Output pin of the build-in VB supply    | • Outputs a voltage (typ. 7.5V) generated in the build-in VB power supply.  
• Provides power from the VB power supply to the input, three-phase distribution, FG, internal clock, over current detection, and other circuits.  
• Connect a capacitor C0 to the CB pin to prevent oscillation. Capacitor with capacity of 0.22µF ±20% is recommended. | 5.3 VB power supply |                                                          |
| 4   | GND   | Control ground pin                      | • It is the ground pin for VCC and VB power lines.                                       |              |                                                          |
| 5   | GH    | Bottom arm reference pin                | • Connected to the external MOS’s source or IGBT’s emitter of the bottom arm.  
• Connected to a shunt resistor Rs to detect over current.  
• The voltage between GH and GND must not exceed the absolute maximum rating. | 5.1 (2) Current limitation |                                                          |
<table>
<thead>
<tr>
<th>No.</th>
<th>Pin</th>
<th>Item</th>
<th>Function and Precaution</th>
<th>Related item</th>
<th>Remark</th>
</tr>
</thead>
</table>
| 6   | NGU   | Bottom arm gate drive       | • Connected to the gate of the external MOS or IGBT of the bottom arm.  
• When connecting a resistor or a capacitor for adjusting the gate switching speed, consider the current consumption and output voltage ringing.                                                                                                                                                                                                                             |              |                         |
|     | NGV   | pin                         |                                                                 |                                                                                           |              |                         |
|     | NGW   |                             |                                                                 |                                                                                           |              |                         |
| 7   | MU    | Top arm reference pin       | • Connected to the output terminals of the external 3-phase inverter bridge.  
• These pins flow the driving current, by the operation of the internal circuit.                                                                                                                                                                                                                                                                                                      | High voltage pin |                         |
|     | MV    |                             |                                                                 |                                                                                           |              |                         |
|     | MW    |                             |                                                                 |                                                                                           |              |                         |
| 8   | PGU   | Top arm gate drive pin      | • Connected to the gate of the external MOS or IGBT of the top arm.  
• When connecting a resistor or a capacitor for adjusting the gate switching speed, consider the current consumption and output voltage ringing.  
• When the component that reduces impedance such as a resistor, a capacitor is connected between PGU and MU (PGV and MV, PGW and MW), the charge pump voltage (VCP) may decrease. For details, see section 5.2.                                                                 | 5.2 Charge pump circuit | High voltage pin       |
|     | PGV   |                             |                                                                 |                                                                                           |              |                         |
|     | PGW   |                             |                                                                 |                                                                                           |              |                         |

**FIGURE 4.2.1 Equivalent Circuit**

**FIGURE 4.2.2 Equivalent Circuit**
<table>
<thead>
<tr>
<th>No.</th>
<th>Pin</th>
<th>Item</th>
<th>Function and Precaution</th>
<th>Related item</th>
<th>Remark</th>
</tr>
</thead>
</table>
| 9   | HUP  | Hall signal input pin        | • Input a Hall signal. The phase switchover is controlled based on the signal.  
• The maximum input voltage is $V_B + 0.5V$. The output voltage of hall element must not exceed the maximum input voltage.  
• If a noise is detected, install a capacitor.  
• Monitoring FG signal is a way to check whether Hall signals are affected by noise or not. Especially, in case of ECN30300, all phase Hall signals can be checked by the way. | Product Specification  
• 4.1 Truth table |        |
| 10  | VSP  | Speed instruction input pin  | • Input a speed instruction signal to generate a PWM signal.  
• Inputting voltage less than all off operation voltage (typ. 1.23V) makes all outputs L  
• If a noise is detected, install a resistor and/or capacitor.  
• 5.4 Power supply sequence  
• 5.5 Output operation  
• 8.1 Electrical static destruction of VSP pin caused by external surge |              |        |

**FIGURE 4.2.3 Equivalent Circuit**

![Equivalent Circuit Diagram](image1)

**FIGURE 4.2.4 Equivalent Circuit**

![Equivalent Circuit Diagram](image2)
<table>
<thead>
<tr>
<th>No.</th>
<th>Pin</th>
<th>Item</th>
<th>Function and Precaution</th>
<th>Related item</th>
<th>Remark</th>
</tr>
</thead>
</table>
| 11  | CR VTR | PWM frequency setting pin   | • Externally connected resistor and capacitor are used to determine the PWM frequency (internal clock).  
  • The frequency is roughly determined by the following equation:  
  \[ f \approx \frac{0.494}{C \times R} \text{ (Hz)} \]  
  | Related item | Remark |  
|     |      |                             | 5.5.1 PWM operation                                                                                                                                                                                                                                                                                                                                 |               |                        |
| 12  | C+ C- CL | Top arm drive circuit power pin  
 Charge pump circuit pin | • Powers the drive circuit for the top arm.  
  • Connect external components (Capacitors and diodes).  
  | Related item | Remark |  
|     |      |                             | 5.2 Charge pump circuit High voltage pin                                                                                                                                                                                                                                                                                                             |               |                        |
| 13  | RS   | Input pin for over current detection signal | • Monitors the voltage of the Rs shunt resistor and detects its over current status.  
  | Related item | Remark |  
|     |      |                             | 5.1 (2) Current limitation                                                                                                                                                                                                                                                                                                                             |               |                        |

**FIGURE 4.2.5 Equivalent Circuit**

**FIGURE 4.2.6 Equivalent Circuit**

**FIGURE 4.2.7 Equivalent Circuit**
<table>
<thead>
<tr>
<th>No.</th>
<th>Pin</th>
<th>Item</th>
<th>Function and Precaution</th>
<th>Related item</th>
<th>Remark</th>
</tr>
</thead>
</table>
| 14  | FG  | Motor rotation speed monitoring pin | • Outputs pulses according to the input signals of the HUP, HUN, HVP, HVN, HWP and HWN.  
• Motor rotation speed can be monitored by measuring the frequency of output pulse. | • 8.2 Electrical static destruction of FG pin caused by external surge | Product Specification  
• 3.2 Time chart |

**FIGURE 4.2.8 Equivalent Circuit**

**FG output pulse**

ECN30300: 3 pulses/period  
ECN30301: 1 pulse/period
5. Functions and operational precautions

5.1 Protection function

(1) Detection of VCC under voltage (LVSD operation)
- When the VCC voltage goes below the LVSD operating voltage (LVSDON), all outputs become L regardless of the input signals.
- This function has hysteresis (Vrh). When the VCC voltage goes up again, the system goes back to a state where the output operates according to the input signals at a level equal to or exceeding the LVSD recovery voltage (LVSDOFF).

![Timing chart for detection of VCC under voltage (LVSD operation)](image)

(2) Current limitation
(a) Operation description
- The system monitors the current flowing through the shunt resistance Rs at the RS pin (see Figure 5.1.2). When the reference voltage for current limitation (Vref = typ. 0.5V) is exceeded, the external IGBTs (or MOSs) of the top or bottom arm are turned off.
- Reset after current limitation is performed in each cycle of the internal clock signal (VTR pin voltage). (See Figure 5.1.3)

![Example of Current of Shunt Resistance](image)
(b) How to set up

- The current limitation setting $IO$ is calculated as follows:
  
  $$ IO = \frac{V_{\text{ref}}}{R_s} $$

  where

  $V_{\text{ref}}$: Reference voltage for current limitation

  $R_s$: Shunt resistor

- In setting a current limit, you should allow for $V_{\text{ref}}$ variance, $R_s$ resistance variance, and the delay between the time the over current limitation is detected and the time the external MOSs or IGBTs are turned off.

- This function is not effective for currents that do not flow forward through the shunt resistor, such as reflux current and power regenerative current (see Figures 5.1.4 and 5.1.5). In practice, users are requested to observe and check the currents (the coil currents of the motor) of the MOSs or IGBTs.
The RS pin contains a filter having a time constant of about 1μs.

If the system malfunctions due to a noise, an effective solution is to add a filter externally. However, beware that the external filter increases the delay time before the external MOSs or IGBTs are turned off.
(d) Precautions on wiring

- Make the wiring of the shunt resistor $R_s$ as short as possible. The GH is connected to the external IGBT emitter or MOS source. If the wiring has a high resistance or inductance component, the IGBT emitter (or MOS source) potential changes, perhaps resulting in the IGBT or MOS malfunctioning.

- Connect the external IGBT emitter or MOS source pins near the pins. If the resistance components of the wiring is poor balanced between the any pins and the shunt resistor $R_s$, the current limit levels in each phase may not be equal.

(e) Motor lock

- This IC does not contain a protection function against motor lock.

- If the motor locks, the phase where the IGBT or MOS turns on is fixed, resulting in a constant current-limited state. This produces a major loss, which results in IGBT or MOS temperature increase and it gets destroyed.

```latex
\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{motor_lock_operation.png}
\caption{Example of Motor Lock Operation}
\end{figure}
```

(3) Protection against short-circuit

- This IC does not contain a protection function against short-circuits (such as load short-circuit, earth fault, and short-circuit between the top and bottom arms).

- The short circuit may cause the destruction of MOSs or IGBTs and the secondary destruction of the IC. Protect them externally.

5.2 Charge pump circuit

5.2.1 Description of operation

- Figure 5.2.1.1 shows a block diagram of a charge pump circuit. The SW1 and SW2 repeat turning on and off alternatively, synchronously with the internal clock.

- When the SW1 is off and the SW2 is on, the CL pin has a potential of 0V. Through the passage (1), charge the capacitor $C_1$.

- Next, the SW1 is turned on and the SW2 is turned off, and the CL pin rises in potential to the $V_S$ level. Through the passage (2), the charge of the capacitor $C_1$ is pumped up to the capacitor $C_2$.

- This operation is repeated with the frequency of the internal clock, and the charge is given to the capacitor $C_2$.

- The capacitor $C_2$ constitutes a power supply for the drive circuit for the top arm.
5.2.2 Charge pump voltage and restriction on the top arm external circuit

(1) The function of the top arm drive power supply
- Power supply to the top arm drive circuit in the IC
- Supply to the output source current of the top arm

(2) Load and power performance
Output source current of the top arm is around 100mA.
However, because of the operation of the charge pump circuit, DC current cannot be sustained.
External MOS / IGBT gate is a capacitive load. Therefore, this circuit has been designed to supply instantaneous current.

(3) The problem with power
DC source current reduces the charge pump voltage. Because top arm drive circuit cannot sustain the operating level, IC may malfunction. It is necessary to limit the current consumed constantly, to sustain a constant level of charge pump voltage.

(4) Circuit operation
Figure 5.2.1.1 shows an example of external circuit consists of Rgs and Cgs. The charge pump voltage is reduced mainly by the Rgs. The charge pump voltage (VCP) must be more than 10V.
As a guide, the Rgs should be more than 10kΩ.

(5) Checkpoints
The charge pump operation and VCC power-up start at the same time.
Check the following items.
1) The charge pump voltage increases with VCC power-up.
2) Control signal (VSP input, etc.) are input after the charge pump voltage is stabilized.

FIGURE 5.2.1.1 Example of Charge Pump and External Circuit
5.3 VB power supply

- The VB power (VB = typ. 7.5V) to be output to the CB pin is generated at the VCC power. The VB power is supplied to the IC internal circuits such as the triangular wave oscillation circuit, over current detection circuit and so on.
- The VB power circuit constitutes a feedback circuit (see Figure 5.3.1). To prevent oscillation, connect a capacitor C0 to the CB pin.
- The recommended capacity for the C0 is 0.22\(\mu\)F ± 20%. If any value other than the recommended one is to be used, refer to the below precautions and determine a suitable capacity.
- The larger the C0 capacity is, the more stable the VB power supply is. It is recommended, however, not to set the capacity figure to an excessive level. As a guide, it should be 2\(\mu\)F to 3\(\mu\)F or less in the non-oscillated region.
- When the current consumption is high, the Vcc voltage may oscillate. Because this can cause VB voltage oscillation, put a capacitor C1 near the VCC pin.

![Fig. 5.3.1 Equivalent circuit for the VB power supply](image)

5.4 Power supply sequence

The order for turning on power supplies should be (1) Vcc, (2) VS, (3) VSP. The order for turning off should be (1) VSP, (2) VS, (3) Vcc. When the order is different from these orders, the external switching devices (MOSs, IGBTs) can be thermally broken.

This is because the saturation voltage of the switching devices may rapidly increase, when gate voltages decrease.

The charge pump voltage (VCP) is used as the power supply of the top arm drive circuit. Input the VSP voltage after the VCP voltage is stabilized.

The rising time of the VCP voltage depends on the external components of the charge pump circuit and the source current of the top arm. Moreover, the source current of the top arm depends on the gate capacitance of the external switching devices and the current consumption of the circuit around the gate. Consider the rising time of the VCP is affected by these parameters.
5.5 Output operation

5.5.1 PWM operation

- PWM signal is generated by comparing the VSP input voltage and triangular signal (CR pin voltage).
- PWM operation is conducted by the top arm and the bottom arm alternately per 60 electrical degrees. (See Figure 5.5.1)
  - VSP input voltage > triangular signal: external switching devices turn on (top or bottom arm)
  - VSP input voltage < triangular signal: external switching devices turn off (top or bottom arm)
- The PWM duty varies linearly between the bottom limit (VSAWL = typ. 2.1V) and the top limit (VSAWH = typ. 5.4V) of the triangular wave amplitude level. It becomes 0% at VSAWL, and 100% at VSAWH. This operation is shown as “PWM1” in the timing chart.

![FIGURE 5.5.1 Timing chart of PWM operation](image)

5.5.2 Overlap operation

The overlap operation is conducted during 30 electrical degree period after 120 degree energization period. The duty of the overlap operation is 1/2 of the PWM1 duty. This overlap operation is shown as PWM2 in the timing chart.

5.5.3 Output all-off function

(a) Function description

- When the input voltage of the VSP pin reaches or goes below the all-off operation voltage (Voff = typ 1.23V), all top and bottom arm outputs become L. The operation of the output with regard to the VSP input voltage conforms to Table 5.5.3.1.

<table>
<thead>
<tr>
<th>VSP input voltage</th>
<th>Top and Bottom Arm Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V ≤ VSP &lt; Voff (typ. 1.23V)</td>
<td>All Arms are L</td>
</tr>
<tr>
<td>Voff (typ. 1.23V) ≤ VSP &lt; VSAWL (typ. 2.1V)</td>
<td>PWM1 &amp; PWM2 periods L</td>
</tr>
<tr>
<td>VSAWL (typ. 2.1V) ≤ VSP</td>
<td>PWM1 &amp; PWM2 periods Active</td>
</tr>
</tbody>
</table>
(b) Precautions

- When the output all-off function is activated while the motor is rotating, a regenerative current is generated in the VS power supply, in some cases resulting in the VS power voltage rise. Keep the VS pin voltage equal to or below the maximum rating. Attention is particularly needed, when the capacity between the VS and GND is small, where the voltage is more likely to rise.

5.6 Internal Filter

- Internal filter circuit is located after the Hall amplifiers and a lap circuit (see Figure 5.6.1). This filter circuit removes the signal and the noise, that width is less than about 0.7 μs (see Figure 5.6.2).
- When the Vcc voltage is dropped by the noise to lower than LVSDON voltage and that width is about 0.7 μs or less, the internal filter is effective.

![FIGURE 5.6.1 Location of the internal filter in the block diagram](image)

![FIGURE 5.6.2 Operation of Internal Filter circuit](image)

5.7 Dead time

- Dead time setting is not required, because the top and bottom arm short circuit mode does not exist for the 150 degree width angle control method of this IC.
### 5.8 External components

#### (1) Standard external components

<table>
<thead>
<tr>
<th>No.</th>
<th>Component</th>
<th>Standard value</th>
<th>Attention on component setting</th>
</tr>
</thead>
</table>
| 1   | C0        | 0.22 μF +/-20% | • USAGE: Filters the internal power supply (VB)  
• Stress voltage is VB (=8.2V) |
|     |           |                | • USAGE: For charge pump  
• Stress voltage is Vcc  
• The following attention is necessary when the standard components are not used.  
  • Vcp is dropped by the internal dissipation current from C+ terminal of IC, when capacity is small.  
  • The voltage impressed to the capacitor becomes VCC in operation. Therefore, the withstand voltage of the capacitor must be more than the VCC voltage.  
• Point to be checked: Note 2 |
| 2   | C1, C2    | 1.0 μF +/-20% | • USAGE: For charge pump.  
• The following attention is necessary when the standard components are not used.  
  • Forward voltage (VF) should be small as much as possible, because large VF reduces Vcp.  
  • Reverse recovery time (trr) should be small as much as possible, because large trr causes Vcp drop.  
  • The withstand voltage of the diode must be more than the VS voltage because CL voltage changes from 0V to VS.  
  • The rush current flows to diode D1 and D2 by charging capacitor C1 and C2 when the VCC power supply is turned on at VS=0V. Select the rated current of the diode in consideration of this current.  
• Point to be checked: Note 2 |
| 3   | D1, D2    | Over 250V, 1A  
trr ≤ 100ns | (Fast Recovery Diode)  
• USAGE: For charge pump.  
• The following attention is necessary when the standard components are not used.  
  • Forward voltage (VF) should be small as much as possible, because large VF reduces Vcp.  
  • Reverse recovery time (trr) should be small as much as possible, because large trr causes Vcp drop.  
  • The withstand voltage of the diode must be more than the VS voltage because CL voltage changes from 0V to VS.  
  • The rush current flows to diode D1 and D2 by charging capacitor C1 and C2 when the VCC power supply is turned on at VS=0V. Select the rated current of the diode in consideration of this current.  
• Point to be checked: Note 2 |
| 4   | Rs        | Note 1         | • USAGE: Sets Over-Current limit  
• Please shorten the wiring between the resistor Rs and the RS pin, and the wiring between the resistor Rs and the GH pin as much as possible.  
• Please shorten the wiring of the external MOS source or IGBT emitter line as much as possible, to prevent the noise to the IC. |
| 5   | CTR       | 1800 pF +/-5%  | • USAGE: Sets PWM frequency  
• Stress voltage is VB (=8.2V)  
• The PWM frequency is approximated by the following equation:  
  \[ \text{PWM Frequency (Hz)} \approx \frac{0.494}{(\text{CTR(f)} \times \text{RTR(Ω)})} \]  
• Please set the maximum frequency of PWM at 20 kHz or less.  
• When the PWM frequency is set at a high frequency, the switching loss is increased. And it produces an increase in temperature of the external MOSs or IGBTs.  
• Please confirm the temperature of external MOSs or IGBTs with an actual set. |
| 6   | RTR       | 22 kΩ +/-5%    | Note 1. The detection current (IO) for the Over Current limit operation can be calculated as follows.  
  \[ \text{IO (A)} = \frac{\text{Vref (V)}}{\text{Rs (Ω)}} \]  
  Where Vref is 0.55V and Rs is a minimum value. (These are worst-case values.)  
  Note 2. When the voltage (Vcp) between C+ and VS is dropped, the gate voltage of top arm MOSs or IGBTs is dropped. And then the loss of MOSs or IGBTs increases. Vcp must not become Vcp<10V. |
(2) Other external components

- Components of Table 5.8.2 are recommended to be arranged to stabilize the power supply and protect IC from voltage surge.
- Please adjust the component setting according to usage conditions. And also, please set up each component close to the terminal of IC to achieve the effect of the voltage surge absorption.

**Table 5.8.2 Other external components**

<table>
<thead>
<tr>
<th>Component</th>
<th>Purpose</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cvcc1</td>
<td>for high frequency noise suppressing</td>
<td>Ceramic capacitor with good frequency response etc.</td>
</tr>
<tr>
<td>Cvcc2</td>
<td>for Vcc power supply smoothing</td>
<td>Electrolytic capacitor etc.</td>
</tr>
<tr>
<td>ZDvcc</td>
<td>for over voltage suppressing</td>
<td>Zener diode with good frequency response etc.</td>
</tr>
<tr>
<td>Cvs1</td>
<td>for high frequency noise suppressing</td>
<td>Ceramic capacitor with good frequency response etc.</td>
</tr>
<tr>
<td>Cvs2</td>
<td>for Vs power supply smoothing</td>
<td>Electrolytic capacitor etc.</td>
</tr>
<tr>
<td>ZDvs</td>
<td>for over voltage suppressing</td>
<td>Zener diode with good frequency response etc.</td>
</tr>
<tr>
<td>Rg1~Rg6</td>
<td>for preventing the high frequency switching of external MOSs or IGBTs</td>
<td>Adjust the resistance depending on the capacity of MOSs or IGBTs.</td>
</tr>
<tr>
<td>Ch1~Ch3</td>
<td>for noise suppressing</td>
<td>Ceramic capacitor with good frequency response etc.</td>
</tr>
</tbody>
</table>

**FIGURE 5.8.1 Block Diagram and external components**
6. Motor control and setting

6.1 Switching Operation in Phase Commutation (Torque Ripple Reduction Control)

- This IC has overlapped energizing period of 30 electrical degrees in phase commutation. Figure 6.1.1 shows an example of Phase-U motor current waveform when the phase is switched from U to V.
- The duty of "PWM2" is about 1/2 against the duty of "PWM1". For instance, the PWM2 duty is 40% when the PWM1 duty is 80%.
- Figure 6.1.2 shows an example of motor current waveform of ECN3030 and ECN3031. They adopt conventional 120-degree commutation method. In this case, the motor current decreases rapidly because the voltage between MU and MW becomes minus after the phase switch.
- On the other hand, the current decreases slowly after the phase switch in Figure 6.1.1. Therefore, the motor torque is smoothed, and the torque ripple is decreased.

![FIGURE 6.1.1 Example for Phase U motor current waveform by ECN30300/30301 Control in phase Commutation from U to V (Stage (4)→(5) in Figure 6.3.1)]

![FIGURE 6.1.2 Example for Phase U motor current waveform by ECN3030/3031 Control in phase Commutation from U to V]
6.2 Cautions about torque ripple reduction control (wide-angle commutation control)

- Overlapped energizing period in phase commutation is set to 30 electrical angle degrees when Hall signal is sine wave. This is achieved by voltage comparison of two signals from Hall signal terminal HUP, HVP, HWP.

- When overlapped energizing period is long, there is a tendency that the reactive current increases and the efficiency decreases; on the other hand, when overlapped energizing period is short, the drastic change in current cannot be suppressed, and torque ripple reduction effect cannot be achieved.

- As a way of prevention, it is necessary to pay attention to following.
  (a) Input Hall signals with minimized sine wave distortion
  (b) Minimize variance of the amplitude and phase of three-phase Hall signals
  (c) Prevent noise in Hall signals

- For example, magnetizing a rotor to generate a sine wave induced voltage, selecting minimum variation Hall elements, and putting a noise elimination capacitors for Hall inputs or similar countermeasures are required.

6.3 Hall element installation position

- Figure 6.3.1 shows an example of an installation position of Hall elements.

- By adjustment of an installation position, the efficiency of a motor and the amplitude of torque ripple can be changed.

- Adjust an installation position by testing with the actual system.

<table>
<thead>
<tr>
<th>Hall Signal Inputs</th>
<th>Output Voltages</th>
</tr>
</thead>
<tbody>
<tr>
<td>HUP–HUN</td>
<td>PGU–MU</td>
</tr>
<tr>
<td>HVP–HVN</td>
<td>NGU–GH</td>
</tr>
<tr>
<td>HWP–HWN</td>
<td>PGV–MV</td>
</tr>
<tr>
<td></td>
<td>NGV–GH</td>
</tr>
<tr>
<td></td>
<td>PGW–MW</td>
</tr>
<tr>
<td></td>
<td>NGW–GH</td>
</tr>
<tr>
<td></td>
<td>FG</td>
</tr>
</tbody>
</table>

Induced voltages:
- U-phase induced voltage
- V-phase induced voltage
- W-phase induced voltage

Stage:
- (12) (1) (3) (5) (7) (9) (11) (2) (4) (6) (8)

FIGURE 6.3.1 Example of Hall Element Installation Position (For Forward Rotation)
6.4 Use for reverse rotation

- Figure 6.4.1 shows timing chart of reverse rotation of a motor. In reverse rotation, there is not an overlap period after phase switch. In this case, the motor current decreases rapidly after the phase switch. Therefore, the effect of torque ripple reduction control is not produced.

![Timing Chart of Reverse Rotation]

6.5 The use of Hall IC

6.5.1 Problems about using Hall ICs

- A motor possibly rotates, if a fixed voltage within the common mode voltage range (3V to VB) is input to HUN, HVN, HWN and Hall IC signals are input to HUP, HVP, HWP.
- However, it is not recommended to use Hall ICs because of the following problems.
  
  - (a) Overlap periods become 60 electrical degrees (See Figure 6.5.1.1) and unstable.
  - (b) Reactive current can be increased and motor efficiency is decreased.
6.5.2 Application example using Hall ICs with additional peripheral circuits

- This is a countermeasure example against problems written in section 6.5.1, which eliminates the overlap periods. The contents in this section show the principle of this example. The operation is not guaranteed. Before applying this, check the operation with a prototype or such.

(1) Input signal pattern
- Table 6.5.2.1 is the truth table in product specification. PWM2 shows the overlap period. When PWM2 periods are changed to L, the operation of the IC becomes 120 degree commutation method. Figure 6.5.2.1 shows input signal pattern example that achieves it.

(2) Circuit example
- Figure 6.5.2.2 shows a circuit example that produces the input signal pattern in Figure 6.5.2.1. The circuit consists of the logic circuits (NOT circuits) to invert signals and resistors to divide voltages, and produces signals based on Hall IC signals. The VB supply (typ. 7.5V) from the IC can be used for the power supply of the circuit. Also in this case, VB power supply output current must be less than 45mA.
- When noise affects the circuit, filter the noise by capacitors, etc..

(3) For reverse rotation
- In Figure 6.5.2.1, the anterior half of 120 degree energization period is PWM1 and the posterior half of it is fixed H. When rotation direction is reverse, the anterior half becomes fixed H and the posterior half becomes PWM1. This may increase torque ripple. Exchanging NOT circuits (IC1, IC2 and IC3) for buffer circuits is a countermeasure example for reverse rotation.
### Table 6.5.2.1 Truth table

<table>
<thead>
<tr>
<th>No.</th>
<th>Stage</th>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>HUP-HUN</td>
<td>HVP-HVN</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TOP</td>
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<tr>
<td></td>
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<td>30300</td>
<td>30301</td>
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<tr>
<td>2</td>
<td>2</td>
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**FIGURE 6.5.2.1 Timing Chart of Application Example using Hall ICs and Additional Peripheral Circuits**
FIGURE 6.5.2.2 Circuit Example using Hall ICs and Additional Peripheral Circuit

6.6 FG output and analog speed signal

- Because the conventional ECN3030 series integrates a MMV (monostable multivibrator) circuit, an analog speed signal can be produced with an external F / V conversion circuit (CR circuit). ECN30300 series does not integrate the MMV circuit. If an analog speed signal is needed, the MMV circuit should be added.
7. Handling Instruction

7.1 Mounting

(1) Insulation between pins
- High voltages are applied between the pins of the numbers specified below. Apply coating or molding treatment.
  - Pin No. 19 ~ 28
  - Coating resin comes in various types. There are some unclear points as to how much thermal and mechanical stresses are exercised on semiconductor devices by size, thickness, and other factors of board shape, and the effects of other components. In selecting coating resin, please consult with your manufacturer.

(2) Connection to N.C pin
- The N.C pin (Pin No. 26) is not connected to the internal IC chip. The potential of the N.C pin is floating. However, the next pins are high voltage pins. If a line is connected to the N.C pin, consider the insulation.

(3) Soldering conditions
- Reflow is recommended for soldering. Figure 7.1.1 shows the reflow condition.
  - FIGURE 7.1.1 Reflow Condition
  - If flow soldering is applied, the peak temperature must be less than 260°C, and the dip time must be less than 10 seconds. Moreover, degradation or destruction is possibly caused by high stress of flow soldering, such as long time thermal stress, mechanical stress, etc. Make sure that your soldering condition does not cause problem as a system.

(4) Use of IC socket
- Because the output current of the IC is more than 100mA, high contact resistance causes noise, etc. This may result in malfunction. Therefore, IC socket should not be used.

7.2 Antistatic measures

- Containers and jigs for transporting ICs should be designed not to get charged under vibration or other impact during transportation. One effective measure is to use a conductive container or aluminum foil.
- Ground all work benches, machines and devices, meters, and other units that may get in contact with the ICs.
- While handling an IC, ground your body with a high resistor (about 100kΩ to 1MΩ) to prevent breakdown due to static electricity that has charged your body and/or clothes.
- Do not produce any friction with other polymer compounds.
- To move any printed circuit board or other component equipped with an IC, make sure that no vibration or friction occurs and short-circuit the pins to keep the potential at the same level.
- The humidity at assembly line to mount the IC on a circuit board should be kept around 45 to 75 percents using humidifiers or such. If the humidity cannot be controlled sufficiently, using neutralization apparatus such as ionizers are effective.
8. Failure Example (Assumptions)

8.1 Electrical static destruction of VSP pin caused by external surge

- **Cause**
  The external surge on the VSP line of the motor was put into IC directly.

- **Phenomenon**
  The VSP signal is not transmitted in IC, and the motor doesn't rotate.

- **Countermeasure**
  The series resistance is inserted so that the external surge is not put into IC directly. In addition, if capacitor is added, it becomes more effective.

![Diagram of VSP pin configuration](image1)

**FIGURE 8.1.1 Example to configuration for external components of VSP**

8.2 Electrical static destruction of FG pin caused by external surge

- **Cause**
  The external surge on the FG line of the motor was put into IC directly.

- **Phenomenon**
  The FG signal of the IC is not output.

- **Countermeasure**
  The buffer circuit using the transistor is used on the motor populated board so that the external surge is not put into IC directly.

![Diagram of FG pin configuration](image2)

**FIGURE 8.2.1 Example of configuration for external components of FG**
8.3 IC destruction by external surge inputted to VS and VCC line (1)

- **Cause**
  The external surge on the VS and VCC line of the motor was put into IC. Because the Zener voltage of the surge suppressor diode was higher than the maximum rating voltage of IC, it did not protect IC.

- **Phenomenon**
  The motor doesn’t rotate by the over voltage destruction of IC.

- **Countermeasure**
  Use the surge suppressor diode of the Zener voltage, which is lower than the maximum rating voltage of IC.

8.4 IC destruction by external surge inputted to VS and VCC line (2)

- **Cause**
  The external surge on the VS and VCC line of the motor was put into IC. Because the capacity of bypass capacitor for surge suppression was small, surge was not able to be suppressed enough.

- **Phenomenon**
  The motor doesn’t rotate by the over voltage destruction of IC.

- **Countermeasure**
  Use the bypass capacitor for surge suppression, which capacity should be enough to suppress surge.

![Small capacity case](image1)

![Large capacity case](image2)

**FIGURE 8.4.1 Example of surge waveform by difference of capacity of bypass capacitor**

8.5 IC destruction by external surge inputted to VS and VCC line (3)

- **Cause**
  The external surge on the VS and VCC line of the motor was put into IC. Because the position of external components for surge suppression on the motor populated board was bad, surge was not able to be suppressed enough.

- **Phenomenon**
  The motor doesn’t rotate by the over voltage destruction of IC.

- **Countermeasure**
  Bypass capacitor and Zener diode for surge suppression should be mounted close to IC.

![Far from IC](image3)

![Close to IC](image4)

**FIGURE 8.5.1 Example of surge waveform by difference of the bypass capacitor location on the board**
8.6 IC destruction by line noise put into VCC (1)

- **Cause**
  Pulsed noise of a voltage that is lower than LVSD level was put into VCC line of IC. In this case, IC repeats short period LVSD operation. Then, external MOSs or IGBTs will have the possibility of causing the overheating destruction.

- **Phenomenon**
  The motor doesn't rotate by the overheating destruction of external MOSs or IGBTs and the over voltage destruction of IC.

- **Countermeasure**
  1. The noise that is put into motor Vcc line is removed by reviewing the power supply circuit (inductance and so on of power cable).
  2. Suppress the noise by mounting the capacitor of enough capacity between Vcc and GND pin of IC. That capacitor should be mounted close to Vcc-GND pin of IC.

![FIGURE 8.6.1 Example of pulsed noise on Vcc](image1)

8.7 IC destruction by line noise put into VCC (2)

- **Cause**
  The surge voltage that exceeds the maximum ratings of IC that was put into VCC pin of IC.

- **Phenomenon**
  The motor doesn't rotate by the over voltage destruction of IC.

- **Countermeasure**
  1. Mount a bypass capacitor C1 close to pin of IC. It's effective to use a capacitor that has excellent frequency characteristics, such as a ceramic capacitor, as a bypass capacitor. As a guide, ones of around 1μF are recommended (The larger the capacity, the more effective it is.).
  2. It is more effective to mount a surge suppression device such as bypass capacitor C2 close to connector of motor populated board like figure 8.7.1.

![FIGURE 8.7.1 Example of surge suppression devices](image2)
8.8 IC destruction by relay noise of inspection machine

- **Cause**
  A mechanical relay for On-off control of electric connection between IC and inspection machine was used. Surge was generated when it was on-off, and it was put into IC.

- **Phenomenon**
  The motor doesn't rotate by the over voltage destruction of IC.

- **Countermeasure**
  Use the wet relay (mercury relay etc.). Confirm surge is not generated when the relay is on-off.

![FIGURE 8.8.1 Example of surge waveform when mechanical relay is used](image)

8.9 Motor failure (missing phase output)

- **Cause**
  The motor has missing phase output that was shipped to the set maker.

- **Phenomenon**
  The motor might start depend on the position of the rotor when starting even if the motor has missing phase output. Therefore, the missing phase output of motor cannot be detected by the motor rotation test.

- **Countermeasure**
  Monitor the Motor current or the torque ripple in order to detect the missing phase output of motor.

![FIGURE 8.9.1 Example of current waveform of the motor that has missing phase output](image)
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