8-channel High Voltage analog switch IC

ECN3290FN Productt Specification Rev.2

ECN3290 is an eight-channel High Voltage analog switching IC on which latch-up free is realized by dielectric isolation technology.
High voltage and low ON-resistance MOS switches are used as output devices controlled by a 5V signal. The ECN3290 is most suited to Ultrasound Imaging applications.

Functions

* High voltage and low on-resistance MOS switches integrated.
* 8bit shift resister integrated.

Features

* Switch on-resistance: 22 Ω typ. (VPP=100V,VNN=-100V,ISIG=5mA, 25ºC)
* Switch breakdown voltage: 220V
* Latch-up free CMOS and High-Voltage drive circuit.
* Power up/down sequence of power supply is free.

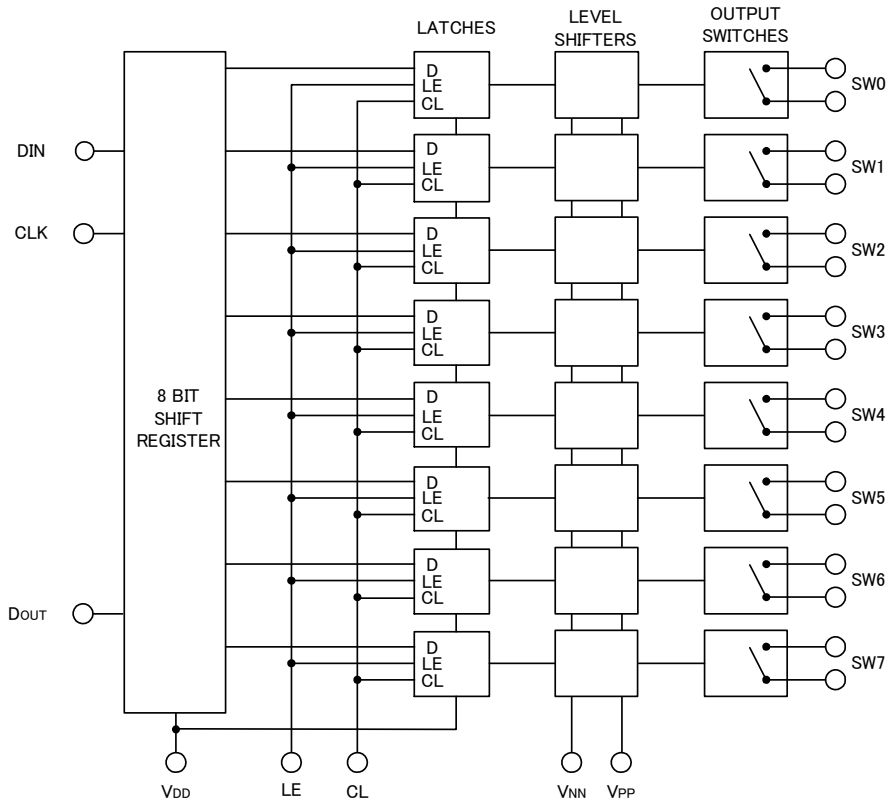


Fig.1 Block diagram

1. General

This Specification shall be applied to the following semiconductor integrated circuit.

1) Parts name : ECN3290FN
2) Application : Ultrasound imaging scanner and others
3) Structure : Monolithic IC
4) Package : QFN28

2. Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Terminal	Values	Unit	Note
1	Logic power supply voltage	VDD	VDD	-0.5 ~ +7V	V	Ta=25ºC
2	VPP-VNN supply voltage	-	VPP, VNN	220V	V	Ta=25ºC
3	VPP Positive high voltage supply	VPP	VPP	-0.5 to VNN+200V	V	Ta=25ºC
4	VNN negative high voltage supply	VNN	VNN	+0.5 to -200V	V	Ta=25ºC
5	Logic input voltages	VDD	DIN, CLK, CL, LE	-0.5 to VDD+0.3	V	Ta=25ºC
6	Analog signal range	-	SW0 to SW7	VNN to VPP	V	Ta=25ºC
7	Operating junction temperature	Tjop	-	-20 to +125	ºC	
8	Storage temperature	Tstg	-	-65 to +150	ºC	
9	Power dissipation	Pw	-	1.2	W	QFN28 Ta=70ºC

3. Electrical Characteristics

3.1 DC Characteristics

Table 2 DC Characteristics Ta=25°C VDD=5V

No.	Items	Symbol	Spec			Unit	Test conditions	
			Min	Typ	Max			
1	Small signal switch on resistance	RONS	-	26	38	Ω	I SIG=5mA	VPP=40V, VNN=-160V
			-	22	27		I SIG=200mA	
			-	22	27		I SIG=5mA	VPP=100V, VNN=-100V
			-	18	24		I SIG=200mA	
			-	20	25		I SIG=5mA	VPP=160V, VNN=-40V
			-	16	25		I SIG=200mA	
2	Small signal switch on resistance matching	ΔRONS	-	5	20	%	VPP=100V, VNN=-100V ISW=5mA	
3	Large signal switch on resistance	RONL	-	20	—	Ω	VPP=100V VNN=-100V	I SIG=1A
4	Switch off leakage per switch	ISOL	-	1.0	10	μA	VSIG=VPP-10V, or VNN+10V	
5	DC offset switch (off)	DCOFF	-	10	100	mV	RL=100kΩ	
6	DC offset switch (on)	DCON	-	10	100	mV	RL=100kΩ	
7	Positive HV supply current	IPPQ1	-	10	50	μA	All SWs off	
8	Negative HV supply current	INNQ1	-	-10	-50	μA	All SWs off	
9	Positive HV supply current	IPPQ2	-	10	50	μA	All SWs on, ISW=5mA	
10	Negative HV supply current	INNQ2	-	-10	-50	μA	All SWs on, ISW=5mA	
11	IPP Supply current	IPP	-	-	7.0	mA	VPP=40V VNN=-160V	50kHz output switching frequency without load
			-	-	5.0		VPP=100V VNN=-100V	
			-	-	5.0		VPP=160V VNN=-40V	
12	INN Supply current	INN	-	-	7.0	mA	VPP=40V VNN=-160V	50kHz output switching frequency without load
			-	-	5.0		VPP=100V VNN=-100V	
			-	-	5.0		VPP=160V VNN=-40V	
13	Logic supply average current	IDD	-	-	4.0	mA	fCLK=5MHz,VDD=5.0V	
14	Logic supply quiescent current	IDDQ	-	-	10	μA		
15	Data out source current	ISOR	0.45	0.70	-	mA	VOUT=VDD-0.7V	
16	Data out sink current	ISINK	0.45	0.70	-	mA	VOUT=0.7V	

3.2 AC Characteristics

Table 3 AC Characteristics Ta=25°C VDD=5V

No.	Items	Symbol	Spec			Unit	Test conditions
			Min	Typ	Max		
1	SW Turn on time	tON	-	-	5.0	μs	VSIG=VPP-10V, RL=10kΩ
2	SW Turn off time	tOFF	-	-	5.0	μs	VSIG=VPP-10V, RL=10kΩ
3	Clock frequency	fCLK	-	-	10	MHz	50% duty cycle, fData=fCLK/2
4	Clock delay time to data out	tDO	30	-	85	ns	DOUT terminal
5	Output voltage spike	+VSPK	-	-	150	mV	VPP=40V, VNN=-160V, RL=50Ω
		-VSPK	-	-	-200		
		+VSPK	-	-	150		VPP=100V, VNN=-100V, RL=50Ω
		-VSPK	-	-	-200		
		+VSPK	-	-	150		VPP=160V, VNN=-40V, RL=50Ω
		-VSPK	-	-	-200		

Table 4 AC Characteristics (for reference purpose only) Ta=25°C VDD=5V

No.	Items	Symbol	Spec			Unit	Condition
			Min	Typ	Max		
1	Off capacitance SW to GND	CSG (off)	-	9	-	pF	0V, 1MHz
2	On Capacitance SW to GND	CSG (on)	-	14	-	pF	0V, 1MHz
3	SW off isolation	KO	-30	-33	-	dB	f=5MHz, 1kΩ//15pF load
			-54	-60	-	dB	f=5MHz, 50Ω load
4	SW Crosstalk	KCR	-54	-60	-	dB	f=5MHz, 50Ω load

Note: These items are not tested when shipped.

4. Recommended Operating Conditions

Please operate in use within the limit of recommended operating conditions detailed in Table 5.

Table 5 Recommended Operating Conditions

No	Items	Symbol	Recommended Value
1	Logic power supply voltage	VDD	4.5V to 5.5V
2	Positive high voltage supply	VPP	40V to VNN+200V
3	Negative high voltage supply	VNN	-40V to -160V
4	High-level input voltage	VIH	VDD - 1.5V to VDD
5	Low-level input voltage	VIL	0V to 1.5V
6	Analog signal voltage peak to peak	VSIG	VNN+10V to VPP-10V
7	Operating free air-temperature	Ta	0°C to 70°C
8	Switching frequency	fsw	50kHz max, Duty Cycle=50%
9	Set up time for LE	tSD	Min.75ns
10	Pulse width of LE	tWLE	Min.75ns
11	Time width of CL	tWCL	Min.60ns
12	Set up time DATA to Clock	tSU	Min.10ns
13	Hold time DATA from Clock	th	Min.20ns
14	Maximum VSIG Slew Rate	dV/dt	Max.30V/ns

Attention ;

1) Power up/down sequence of power supply is arbitrary except GND terminal of IC must be powered-up first and powered-down last.
2) It is indispensable to make there are not to exceed a maximum rated voltage by the occurrence of the excessive voltage in case of investing and cutting of the power supply.

5. Test Circuit

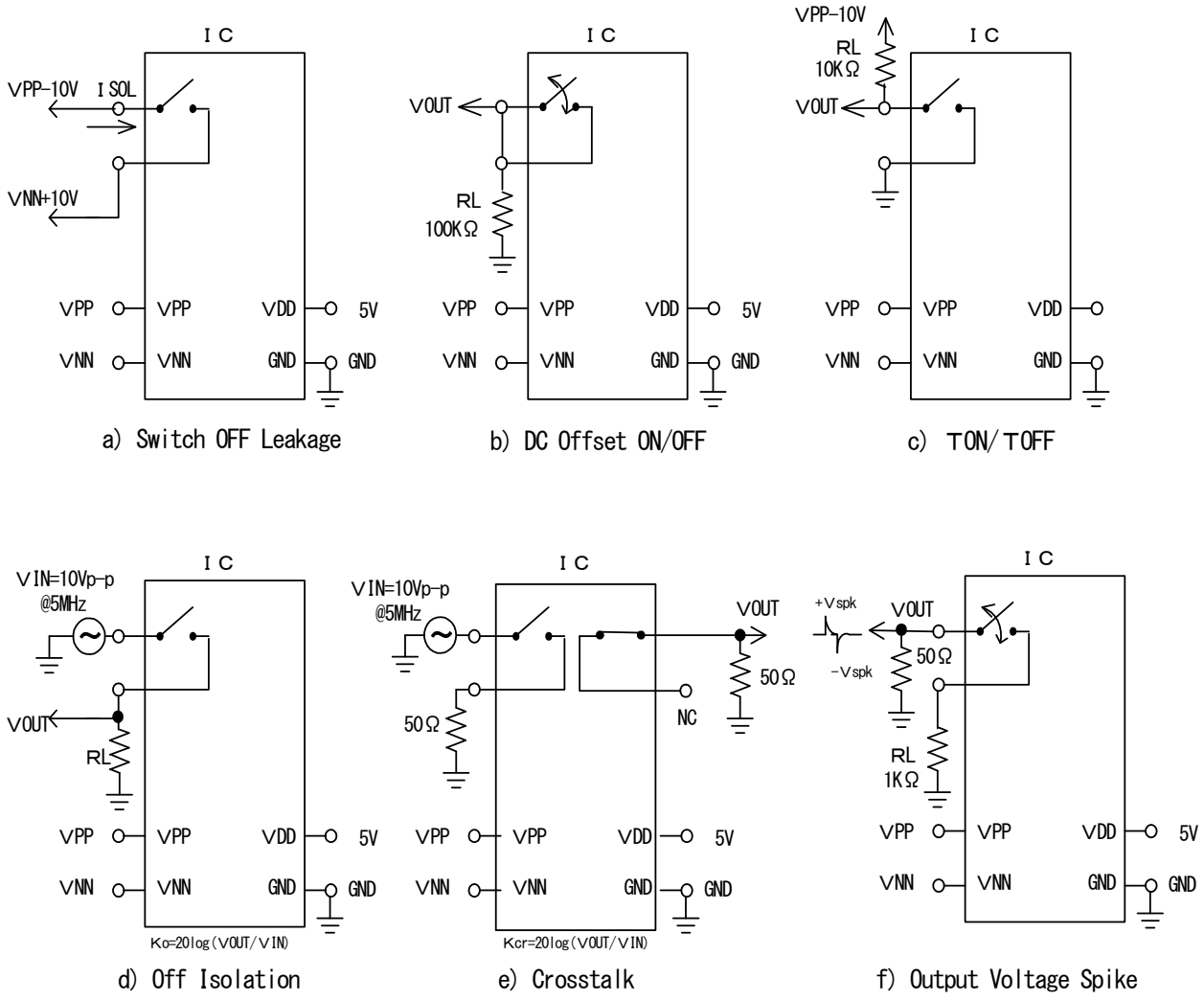


Fig. 2 Test Circuit

6. Timing Waveforms

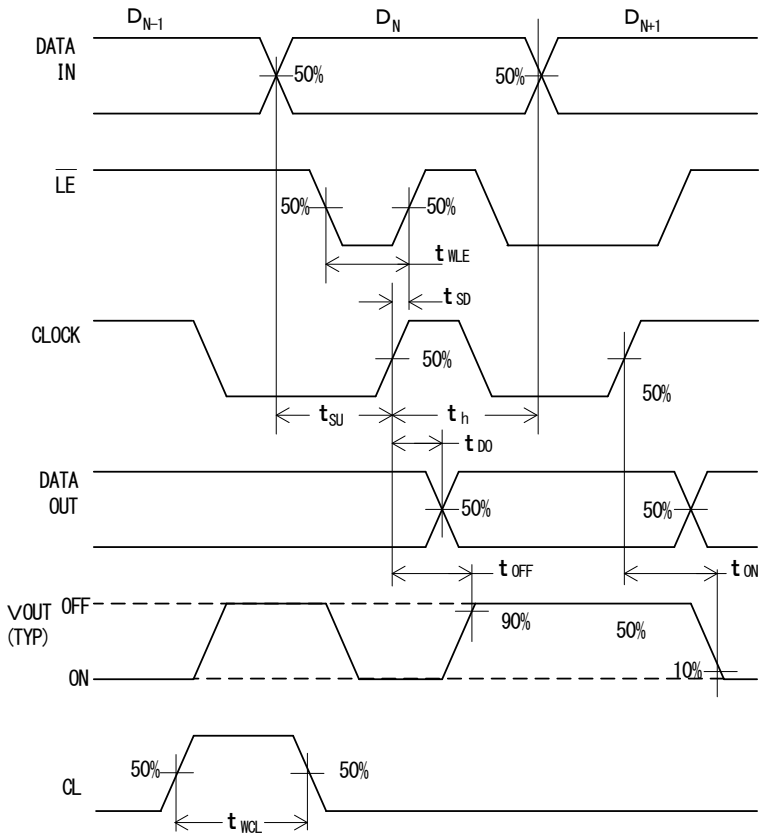


Fig. 3 Timing Waveforms

7. Truth Table

Table 6 Truth table

D0	D1	D2	D3	D4	D5	D6	D7	LE	CL	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	Hold previous state							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

8. Pin Configuration

Table 7 Pin Configurations

Pin	Functions	Pin	Functions
1	SW5	15	N/C
2	SW4	16	VNN
3	SW4	17	GND
4	SW3	18	VDD
5	SW3	19	DIN
6	SW2	20	CLK
7	N/C	21	$\overline{\text{LE}}$
8	SW2	22	CL
9	SW1	23	DOUT
10	SW1	24	SW7
11	SW0	25	SW7
12	SW0	26	SW6
13	N/C	27	SW6
14	VPP	28	SW5

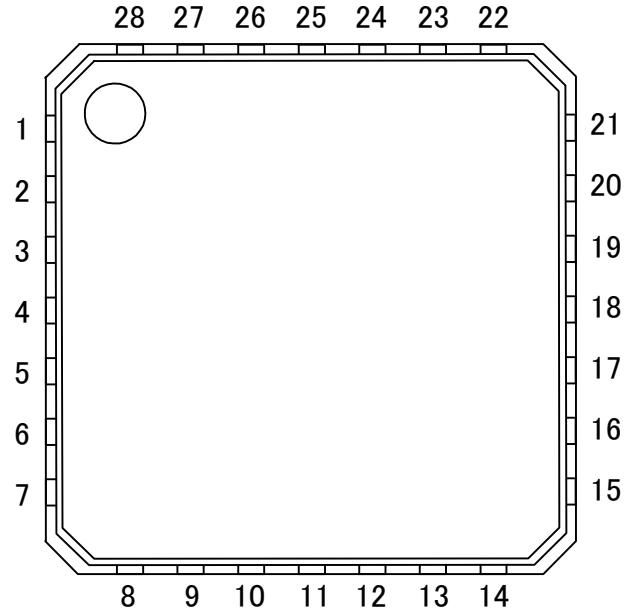


Fig.4 Package Dimensions (Quad Flat No-Lead 28pin)

9. Package Outline

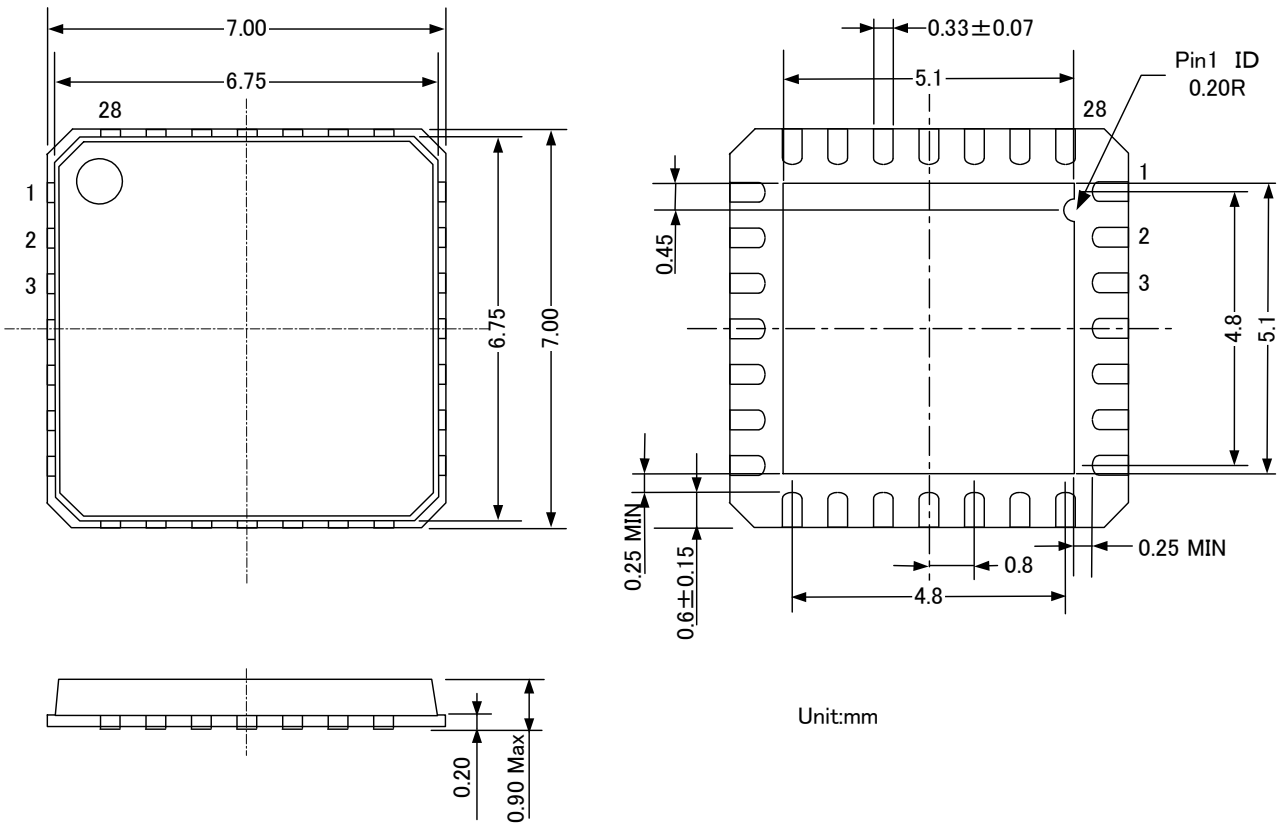


Fig.5 Package Outline (Quad Flat No-Lead 28pin)

Note ;

QFN28(Quad Flat No-Lead 28 Pin) Package

a) Connection of tab

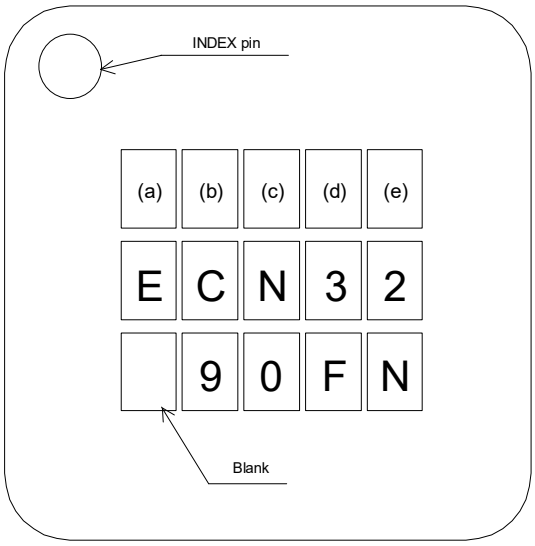
A tab of the back of a QFN package and each terminal of IC are not connected. Please use the tab as open, or use it for GND, connecting.

Do not impress the voltage beyond 220V of a rated value between a tab and each terminal of IC.

b) Pb free

Solder plating of the terminal of a QFN package and a back tab has adopted SnBi plating.

10. Marking spec



Lot numbering rule

(a) :Year code (Least significant digit of Assembled year (A.D.))

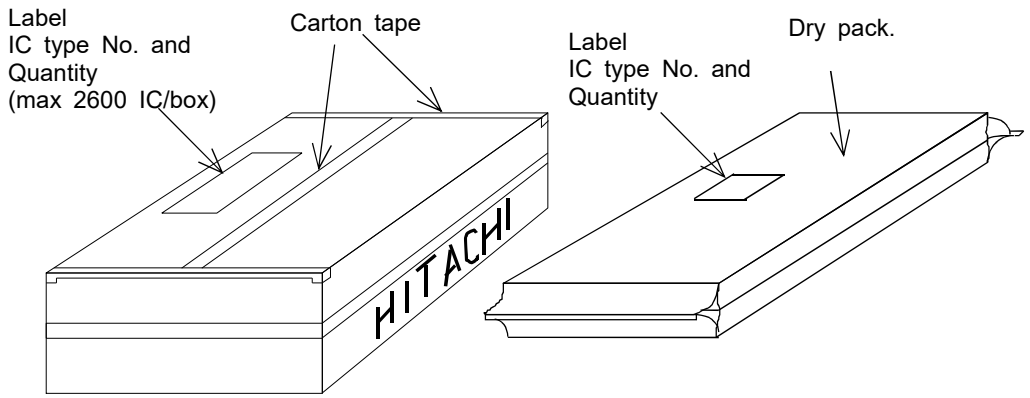
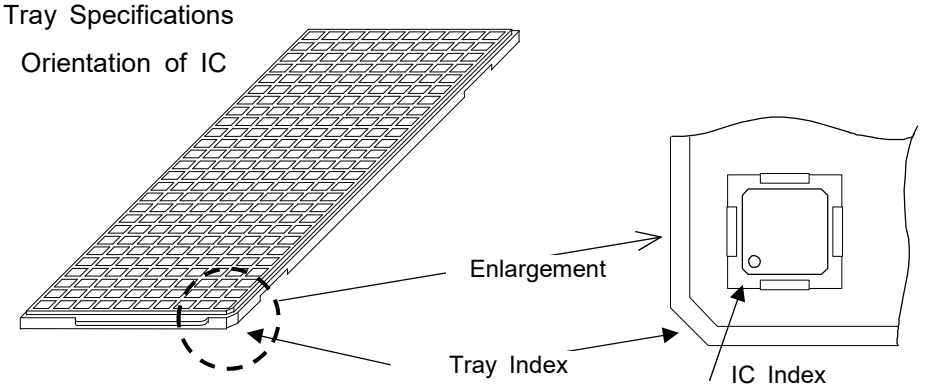
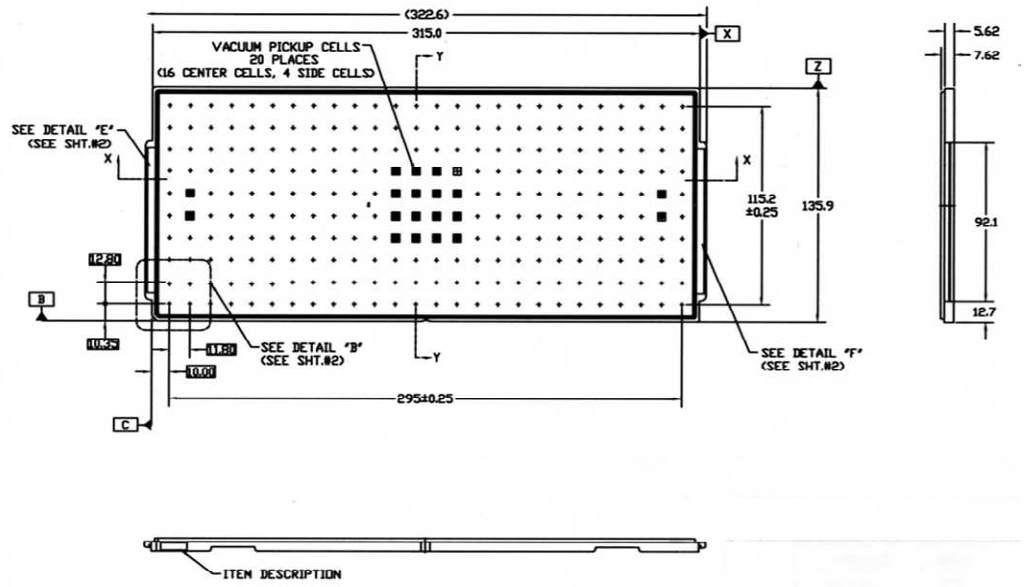
(b) :Month code (Refer to following table.)

Month	1	2	3	4	5	6	7	8	9	10	11	12
Month code	A	B	C	D	E	K	L	M	N	X	Y	Z

(c),(d),(e) :Serial number within year/month code

11. Packing Form

Packaging details are as shown below.

1.Outer and inner packing	 Outer box (cardboard box) Inner
2.Tray	Tray Specifications Orientation of IC  Tray dimension  (1) Material of tray is MPPO containing carbon and static proof. (2) Packing quantity is max 260 IC/Tray. (3) Maximum heat resistant temperature is 150deg , 24h.

12. Inspection

Hundred percent inspection shall be conducted on electric characteristics.

13. Important Notice

13.1 Hitachi warrants performance of its power semiconductor products (hereinafter called “products”) to the specifications applicable at the time of sale in accordance with the Product Specification. Testing and other quality control techniques are utilized to the extent Hitachi needs to meet specifications described in the Product Specification. Specific testing of all parameters of each device is not necessarily performed, except those mandated by related laws and/or regulations.

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14. Cautions

14.1 Customers are advised to follow the below cautions to protect semiconductor from electrical static discharge (ESD).

a) IC needs to be dealt with caution to protect from damage by ESD. Material of container or any device to carry semiconductor devices should be free from ESD which may be caused by vibration while transportation. To use electric-conductive container or aluminum sheet is recommended as an effective countermeasure.

b) Those what touch semiconductor devices such as work platform, machine and measuring and test equipment should be grounded.

c) Workers should be grounded connecting with high impedance around 100kΩ to 1MΩ while dealing with semiconductor to avoid damaging IC by electric static discharge.

d) Friction with other materials such as a high polymer should not be caused.

e) Attention is needed so that electric potential will be kept on the same level by short circuit terminals when PC board with mounted IC is carried and that vibration or friction might not occur.

f) Air conditioning is needed so that humidity should not drop.

14.2 Refer to “Precautions for Use of High-Voltage Monolithic ICs” for the other precautions and instructions on how to deal with products.

14.3 Regardless of changes in external conditions during use, “absolute maximum ratings” should never be exceeded in designing electronic circuits that employ products. In a case absolute maximum ratings are exceeded, products may be damaged or destroyed. In no event shall Hitachi be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.

14.4 Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure.

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In such cases it is advised customers ensure circuit and/or product safety by using semiconductor devices that assures high reliability or by means of user’s fail-safe precautions or other arrangement. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

Precautions for Safe Use and Notices

If semiconductor devices are handled in an inappropriate manner, failures may result. For this reason, be sure to read the latest version of “Instructions for Use of Hitachi High-Voltage Monolithic ICs” before use.

This mark indicates an item requiring caution.

CAUTION This mark indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury and damage to property.

CAUTION

(1) Regardless of changes in external conditions during use of semiconductor devices, the “maximum ratings” and “safe operating area(SOA)” should never be exceeded when designing electronic circuits that employ semiconductor devices.

(2) Semiconductor devices may fail due to accidents or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy and measures to prevent misuse, in order to avoid extensive damage in the event of a failure.

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