ECN3018 HITACHI

Brushless DC (BLDC) Single-Chip Motor Drive IC

The ECN3018 is a fully integrated, single-chip BLDC motor driver that facilitates a rapid design process and low part count solution. The chip integrates BLDC Logic with a 3-Phase Inverter containing six (6) 250V rated IGBTs and a Charge Pump TOP Arm bias. To reduce motor current losses, a BLDC motor can now be driven directly from rectified 110VAC (up to 185VDC) power lines. On-Chip Brushless (electronic) commutation logic is fully integrated with analog OSC/PWM functions that permit an analog (VSP) voltage to control motor speed.

Description

- Integrated, Single-Chip Direct BLDC Motor Driver IC
- Integrated 3-Phase BLDC motors operating from a 185VDC (down to 20VDC) voltage bus
- Integrated Charge Pump - Creates constant TOP Arm bias independent of motor speed
- Integrated 3-Phase Brushless (Electronic) commutation via external Hall ICs
- Integrated 3-Phase 6-IGBT Motor Bridge with on-chip free-wheeling diodes
- Latch-Up free monolithic IC built with a high voltage Dielectric Isolation (DI) process
- Available in 3 package types with built-in heat sink (Tab)

Functions and Features

- Simple Variable Speed Control via a single (VSP) analog input
- PWM Speed Control without requiring a MicroController
- PWM duty cycle generator provides a 0% to 100% speed control range
- Tachometer - Generates a (RPM/60)**x**(P/2) **x** 3 Hertz speed signal (FG)
- BOTTOM Arms switch at up to 20kHz via an on-chip OSC/PWM
- On-Chip 7.5VDC regulator (CB) with a guaranteed Min load (25mA)
- Over-Current protection is set by an external Sense Resistor (RS)
- Under-Voltage protection for TOP and BOTTOM IGBT Arms

Block Diagram

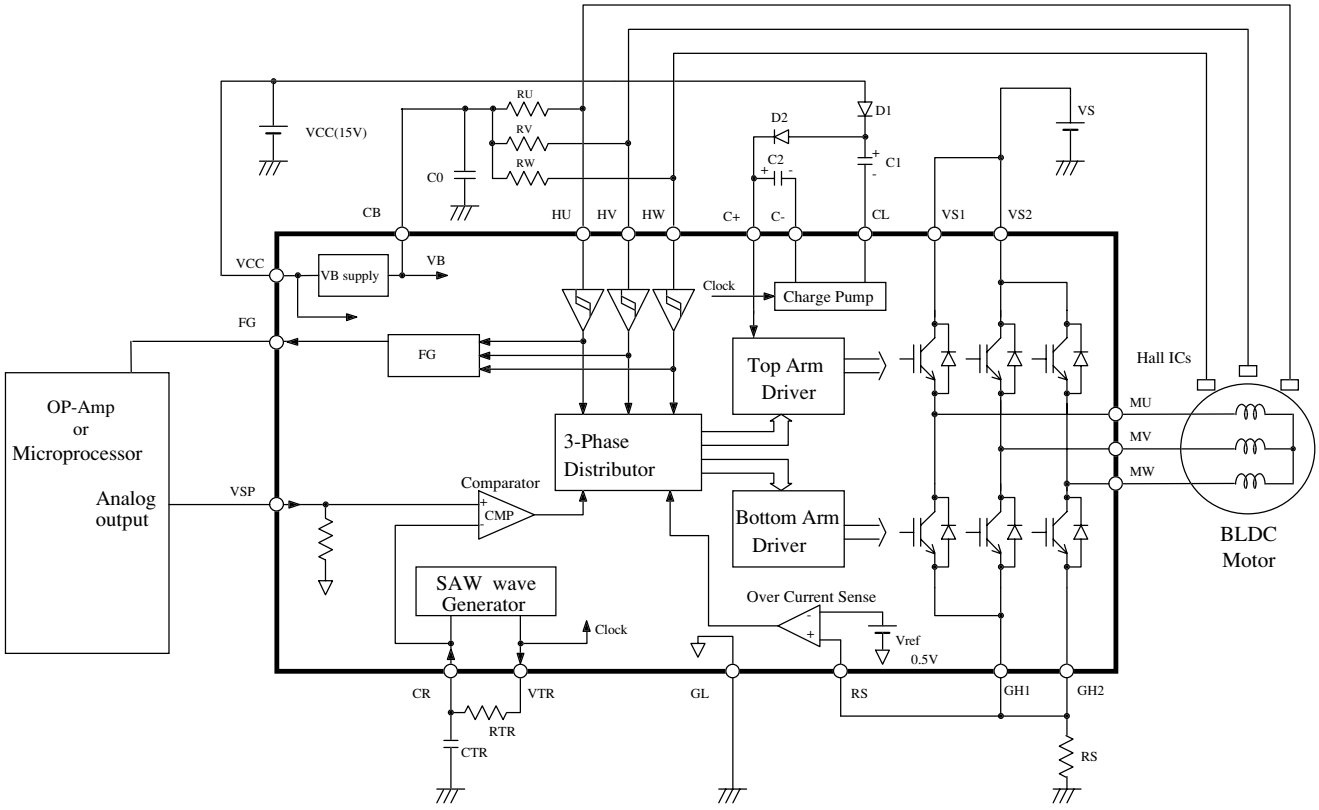
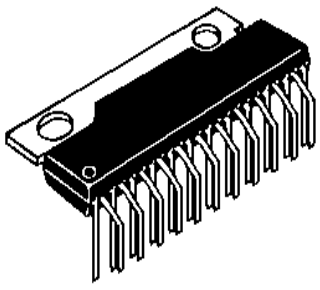


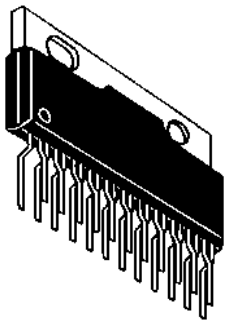
Figure 1 Block Diagram

NOTE: A Speed Reverse Function for Single Chip BLDC Motor Drive ICs (such as this ECN3018) is discussed in Motor Control Tech Tips, Volume 1, Issue 9 (Oct '02). "Implementing Single Chip Safe Direction Reversal and TACH Pulse" (see our web pages).

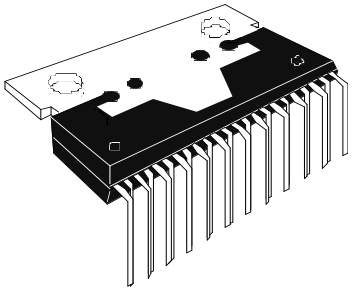
Part Names and Packaging



ECN3018SP
(Package Type:SP-23TA)



ECN3018SPV
(Package Type:SP-23TB)



ECN3018SPR
(Package Type:SP-23TR)

1. Maximum Allowable Ratings

T a = 25 °C

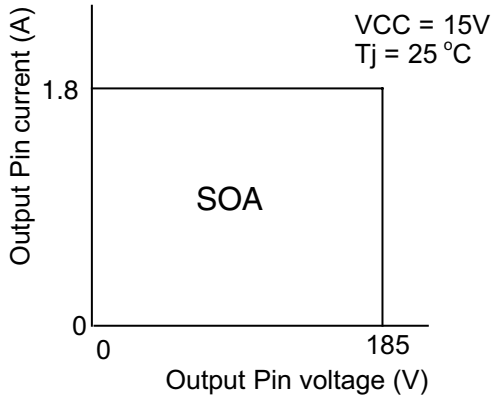
No.	Items	Symbols	Terminal	Ratings	Unit	Condition
1	Output Device Breakdown Voltage	VSM	VS1,VS2 MU,MV,MW	250	V	
2	Supply Voltage	VCC	VCC	18	V	
3	Input Voltage	VIN	VSP,RS HU,HV,HW	-0.5 ~ VB+0.5	V	
4	Output Current	IOM	MU, MV, MW	1.8	A	Note 1
5	Operating Junction Temperature	Tjop		-20 ~ +135	°C	Note 2
6	Storage Temperature	Tstg		-40 ~ +150	°C	

General Note: Please refer to the “Precautions for Use” on our website.

Note 1: The Derating Design Standards (see Table 1.1, Page 1 of “Precautions for Use” on our website) allows 1.4A Peak and 0.9A Average motor currents.
Note 2: Thermal resistance
1) Between junction and IC case (Tab): Rj-c = 4 °C/W
2) Between junction and air: Rj-a = 40 °C/W

1.1 Safe Operating Area (SOA) and Derating

The ECN3018 should never be used outside the SOA shown, where the current and voltage are at the MU, MV and MW pins (motor coils) when the phase is changed (turned-OFF).



2. Recommended Operating Conditions (Tj < 110 °C)

No.	Items	Symbols	Terminal	MIN	TYP	MAX	Unit	Condition
1	Supply Voltage	VS	VS1, VS2	50	141	185	V	
2		VCC	VCC	13.5	15	16.5	V	
3	Supply Current	IS	VS1, VS2	-	0.7	1.0	A	Notes 1, 2

Note 1. Supply current means average supply current including motor Start and Speed-Up currents. Motor current transients (during Start & Speed-Up) may require a Soft-Start circuit to limit these initial currents, see:
Motor Control Tech Tips, Volume 1, Issue 1 (Feb’02), “Motor Soft-Start” (see our web pages).
Motor Control Tech Tips, Volume 1, Issue 7 (Aug’02), “BLDC Power BUS Under/ Over Voltage Protection” (see our web pages).
Note 2. Recommended Minimum external RS value : RS = 0.55Ω

3. Electrical characteristics

Suffix: T = Top arm, B = Bottom arm Ta= 25°C Unless otherwise specified, VCC =15V, VS = 141V

No.	Items	Symbols	Terminal	MIN	TYP	MAX	Unit	Condition
1	Standby Current	IS	VS1, VS2	-	4.0	10	mA	VSP=0V
2		ICC	VCC	-	10	20	mA	
3	Output device FVD	VFT	MU,MV,MW	-	2.0	3.0	V	I=0.7A
4		VFB	MU,MV,MW	-	2.0	3.0	V	
5	Turn ON	TdONT	MU,MV,MW	-	0.5	3.0	µs	
6	Delay Time	TdONB	MU,MV,MW	-	0.5	3.0	µs	I=0.7A
7	Turn-OFF	TdOFFT	MU,MV,MW	-	1.0	3.0	µs	Resistance Load
8	Delay Time	TdOFFB	MU,MV,MW	-	0.8	3.0	µs	
9	Free Wheel	VFDT	MU,MV,MW	-	2.0	2.5	V	I=0.7A
10	Diode FVD	VFDB	MU,MV,MW	-	2.2	2.7	V	
11	Output Resistance	RVTR	VTR	-	200	400	Ω	
12	H or L Level of	VSAWH	CR	4.9	5.4	6.1	V	Note 1
13	SAW wave	VSAWL	CR	1.7	2.1	2.5	V	
14	Amplitude of SAW wave	VSAWW	CR	2.8	3.3	3.8	V	Note 2
15	Reference Voltage	Vref	RS	0.45	0.5	0.55	V	
16	Hall signal	VIH	HU,HV,HW	3.5	-	-	V	
	Input Voltage	VIL	HU,HV,HW	-	-	1.5	V	
17	Hall signal Input Current	IIL	HU,HV,HW	-100	-	-	µA	HU,HV,HW=0V Note 3 Pull Up Resistance
18	Input Current at VSP	IVSPH	VSP	-	-	50	µA	VSP=5.0V Note 4 Pull Down Resistance
19	Offset Voltage at VSP	SPCOMOF	VSP	-40	10	60	mV	against CR
20	VB Output Voltage	VB	CB	6.8	7.5	8.2	V	
21	VB Output Current	IB	CB	25	-	-	mA	$\delta V_{LOAD} < -0.1V$
22	FGOutput Resistance	RFGP	FG	-	1.5	3.0	k Ω	IFG = 1mA Note 5
23		RFGN	FG	-	0.7	1.5	k Ω	IFG =-1mA Note 5
24	LVSD Output Voltage	LVSDON	VCC, MU, MV,MW	10.0	11.5	12.9	V	Note.6
25	LVSD recover Voltage	LVSDOFF		10.1	12.0	13.0	V	
26	LVSD reset hysterisis	Vrh		0.1	-	0.9	V	

Note 1. See Standard Applications in Section 5, page 8 to set the SAW wave frequency.

Note 2. The amplitude of SAW (i.e., VSAWW) is determined by the following equation:

VSAWW = VSAWH – VSAWL

Note 3. Internal Pull Up resistors are typically 200 kΩ. The equivalent circuit is shown in Fig. 2.

Note 4. Internal Pull Down resistors are typically 200 kΩ. The equivalent circuit is shown in Fig. 3.

Note 5. The equivalent circuit is shown in Fig. 4.

Note 6. The LVSD (Low Voltage Shut Down) function Detects and Shuts-Down at lower VCC.

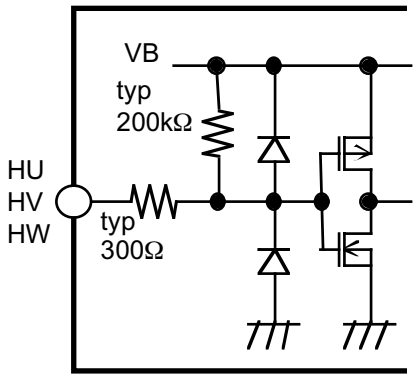


Figure 2 Equivalent circuit around HU, HV, HW

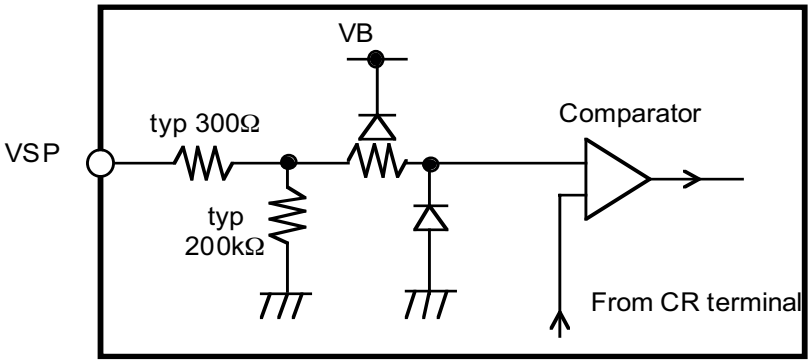


Figure 3 Equivalent circuit around VSP

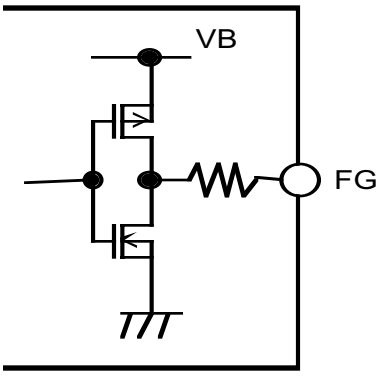


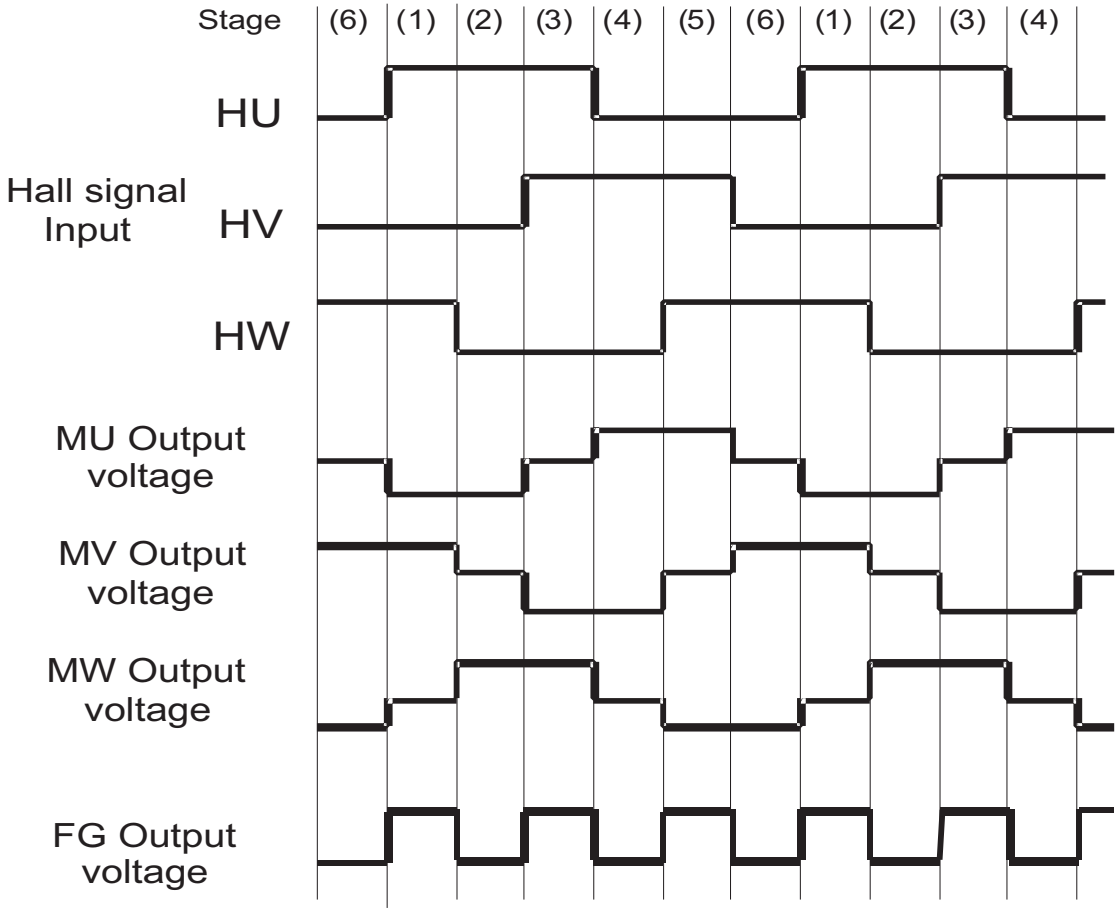
Figure 4 Equivalent circuit around FG

4. IGBT Motor Bridge Commutation and Logic Functions

4.1 Truth table

stage	Hall signal Input			U		V		W		FG Output
	HU	HV	HW	Top arm	Bottom arm	Top arm	Bottom arm	Top arm	Bottom arm	
(1)	H	L	H	OFF	ON	ON	OFF	OFF	OFF	H
(2)	H	L	L	OFF	ON	OFF	OFF	ON	OFF	L
(3)	H	H	L	OFF	OFF	OFF	ON	ON	OFF	H
(4)	L	H	L	ON	OFF	OFF	ON	OFF	OFF	L
(5)	L	H	H	ON	OFF	OFF	OFF	OFF	ON	H
(6)	L	L	H	OFF	OFF	ON	OFF	OFF	ON	L
-	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	L
-	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	H

4.2 Timing chart



4.3 PWM operation

The PWM signal is generated by comparing the input voltage at the VSP pin with an internal SAW wave voltage (available at the CR pin). The Duty Cycle of the resulting PWM signal is thus directly, linearly controlled by VSP pin voltage: from the Min of VSAWL to the Max of VSAWH. That is, when VSP is below VSAWL, the PWM duty cycle is at the Minimum value of 0%. When VSP is above VSAWH, the PWM duty is at the Maximum value of 100%. ECN3018 operates in 2 quadrants by chopping the BOTTOM Arms with this PWM duty cycle during the appropriate commutation times (phases). Thus, the duty cycle controls motor torque and speed.

4.4 Motor Over-Current limiting operation

Over-Current is monitored via the voltage drop across an external resistance RS. If the input voltage at the RS pin exceeds the internal Reference voltage (Vref is typically 0.5V), all BOTTOM Arms are Turned-OFF. Following an Over Current event, reset is automatically attempted during each period of the on-chip OSC. This on-chip OSC signal is available at the VTR pin. If the Over-Current function is not used, the RS pin must be connected to the GL pin with less than 100Ω.

4.5 VCC Under-Voltage Detection

If VCC drops below LVSDON (11.5V typ), all IGBTs TOP and BOTTOM Arms Turn-OFF. Normal operation returns when VCC rises above LVSDOFF: the value of LVSDOFF is LVSDON + Vrh.

5. Standard application

5.1 External components

Components	Standard value	Usage	Remarks
C0	0.22μF ± 20%	Filters the internal power supply (VB)	Stress voltage is VB (=8.2V)
C1, C2	1.0μF ± 20%	The Charge Pump	Stress voltage is VCC
D1, D2	Hitachi DFG1C4 (Glass mold type), DFM1F4 (Resin mold type) or equivalent	The Charge Pump	400V, 1A trr ≤ 100ns
RS	Note 1	Sets Over-Current limit	
CTR	1800 pF ± 5%	Sets PWM frequency	Stress voltage is VB (=8.2V) Note 2
RTR	22 kΩ ± 5%	Sets PWM frequency	Stress voltage is VB (=8.2V) Note 2

Note 1: Peak Start-Up current (IO) is fixed by the Over-Current limit detection/protection function. This requires the user to provide a sense resistor (RS) scaled to detect the desired Peak Start-Up current. The value of RS can be calculated by substituting the maximum Vref value (0.55V) and the Peak current desired. Recognize that the resultant value of RS is the minimum value of the required resistor, which is the worst case value.

RS = Vref / IO

Where: IO is in Amps, Vref = 0.55V and RS is the low tolerance value of the required resistor.

Since this triggers Over-Current protection, IO represents the Peak (MAX) desired current in a given design.

Note 2: The PWM frequency is approximated by the following equation:

FPWM (in Hertz) ~ 0.494 / (CTR **x** RTR) … Note: CTR is in Farads, RTR is in Ohms

Note 3: A standard value for the Hall resistors RU, RV, RW is 5.6 kΩ ± 5%

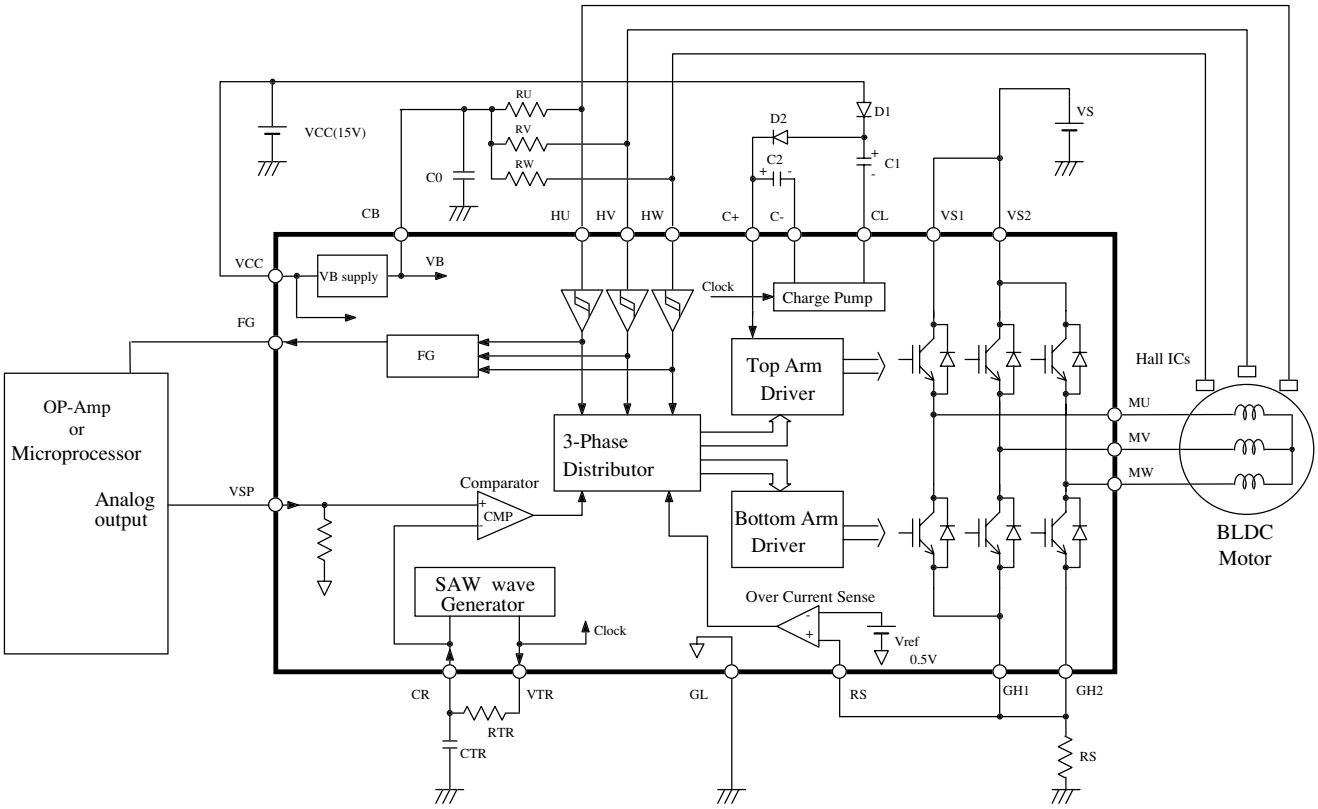


Figure 5. Block Diagram

NOTE: A Speed Reverse Function for Single Chip BLDC Motor Drive ICs (such as this ECN3018) is discussed in Motor Control Tech Tips, Volume 1, Issue 9 (Oct '02). "Implementing Single Chip Safe Direction Reversal and TACH Pulse" (see our web pages).

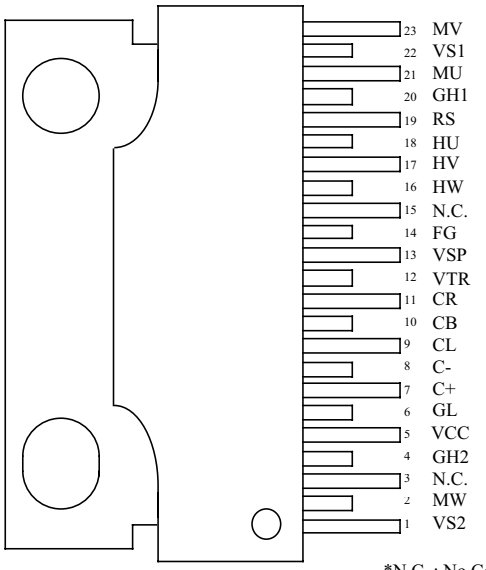
5.2 Input Pins

In some applications, input pins may be noise sensitive due to their high impedance. This can be minimized with the use of external resistance and/or capacitance as follows:

- A pull down resistor of 5.6 kΩ ± 5% from the VSP pin to ground (the GL pin).

- A 500 pF ± 20% ceramic capacitor from HU, HV, HW and VSP pins to ground (the GL pin).

6. Pinout



(Marking side)

*N.C. ; No Connection

7. Pin Definitions

Terminal No.	Symbol	Definition	Remarks
1	VS2	Power Supply for Upper IGBT of phases V and W	Note1, Note2
2	MW	W phase output (to BLDC motor coil W)	Note1
3	NC	No Connection	Note4
4	GH2	W phase emitter of IGBT and anode of FWD. Connect RS	Note3
5	VCC	Analog power supply	
6	GL	Analog ground	
7	C+	For the Charge Pump circuit, power supply for TOP Arm drive circuit	Note1
8	C-	For the Charge Pump circuit	Note1, Note2
9	CL	For the Charge Pump circuit	Note1
10	CB	Internally regulated (VB) power supply output	
11	CR	Connect resistance & capacitance to generate the PWM clock frequency	
12	VTR	Connect resistance to generate the PWM clock frequency	
13	VSP	Input analog voltage that varies the PWM duty cycle from 0% to 100%	
14	FG	Tachometer output signal whose frequency is (RPM/60)**x**(P/2)**x**3 Hertz	
15	NC	No Connection	Note4
16	HW	Input signal from the Hall IC of phase W	
17	HV	Input signal from the Hall IC of phase V	
18	HU	Input signal from the Hall IC of phase U	
19	RS	RS voltage detect input for the on-chip Over Current limit detection	
20	GH1	U and V phase emitters of IGBT and anode of FWD. Connect RS.	Note3
21	MU	U phase output (to BLDC motor coil U)	Note1
22	VS1	Power Supply for Upper IGBT of phase U	Note1, Note2
23	MV	V phase output (to BLDC motor coil V)	Note1

Note1: This is a High Voltage pin.
Note2: The VS1, VS2 and C- pins are connected within the IC but, VS1 and VS2 must both be connected to the VS Supply Voltage by external wiring.
Note3: GH1 and GH2 are not connected within the IC and must be connected by external wiring.
Note4: Not connected

8. Quality Assurance

8.1 Appearance and dimension
ANSI Z1.4-1993 General inspection levels II AQL 1.0%
8.2 Electrical characteristics
ANSI Z1.4-1993 General inspection levels II AQL 0.65%

9. Do's and Don'ts

9.1 The tab should be attached to a heat sink by applying a torque of 0.39 to 0.78 N-m.

9.2 The tab should not be soldered.

9.3 To protect this chip from Electrical Static Discharge (ESD), the ECN 3018 should be handled in accordance with normal industry standard procedures for protection against damage due to ESD. For a more detailed discussion of this area, please refer to the web, "Precaution for Use" Section 5.

9.4 Depending on local industry/market regulations, conformal coating may be required for the following pin-to-pin spacings: 1-2, 2-4, 6-7, 8-9, 9-10, 20-21, 21-22, 22-23.

9.5 Protective function against short circuit (ex. load short, line-to-ground short or TOP/BOTTOM Arm shorts) is not built into this IC. External protection may be needed to prevent IC breakdown under these potential application conditions.

9.6 Hitachi high voltage ICs are manufactured to meet standard industrial grade reliability specifications. In cases where extremely high reliability is required (such as nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment) system integrity must be achieved via fail-safe system design. Additionally, it is the responsibility of the designer to insure that any IC failure does not damage property or human life. Users should evaluate and consider employing the following design precautions:

a) Sufficient derating of the specifications should be utilized to minimize the possibility of failures based on the maximum ratings, operating temperature and environmental conditions.

b) Design redundancy should be applied so that application performance will be maintained even in a case of IC failure.

c) The system design should implement fail-safe design techniques to protect property and human life even where incorrect system operation is experienced.

10. Precautions for Safe Use

If semiconductor devices are handled in an inappropriate manner, failure may result. For this reason, be sure to read “Precautions for Use” on our website before use.

⚠ CAUTION

(1). Regardless of changes in external conditions during use, “absolute maximum ratings” should never be exceeded in designing electronic circuits that employ semiconductors.
Furthermore, in the case of pulse use, “safe operating area (SOA)” precautions should be observed.

(2). Semiconductor devices may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features and practices, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of failure.

(3). In cases where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support related medical equipment, fuel control equipment and various kinds of safety equipment), safety should be ensured by using semiconductor devices that feature assured safety or by means of user’s fail-safe precautions or other arrangement. Or consult Hitachi’s sales department staff.

(If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

11. Notices

1. This publication contains the specifications, characteristics (in figures and tables), dimensions and handling notes concerning power semiconductor products (hereinafter called “products” to aid in the selection of suitable products.

2. The specifications and dimensions, etc. stated in this publication are subject to change without prior notice to improve product’s characteristics. Before ordering, purchasers are advised to contact Hitachi’s sales department for the latest version of this publication and specifications.

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Appendix - Supplementary and Reference Data

Refer to the derating information below when designing with the ECN3018.
This information is provided for reference purposes only.

1. Safe Operating Area (SOA) Design Margin

1.1 SOA

The ECN3018 should never be used outside the SOA shown below.
The following figure is an evaluation of the SOA. Tj < 110 °C.
IM and VM are the Current and Voltage measured at ECN3018 pins at the change of phase (Turn ON and turn OFF).

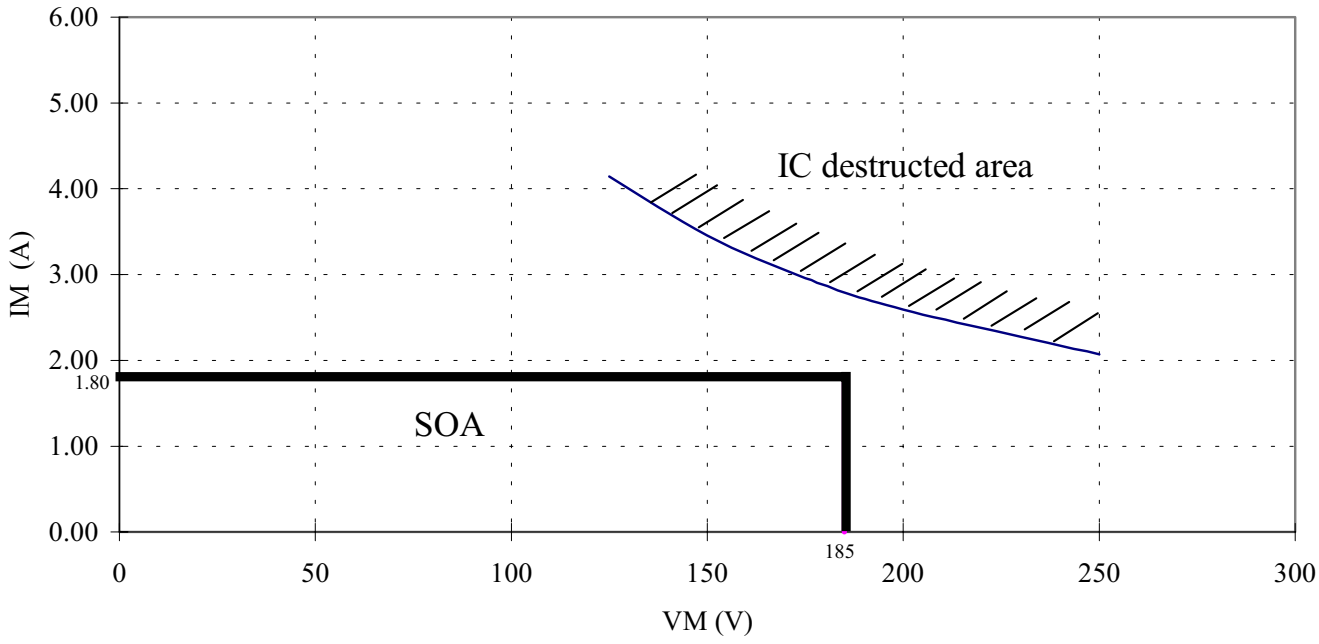
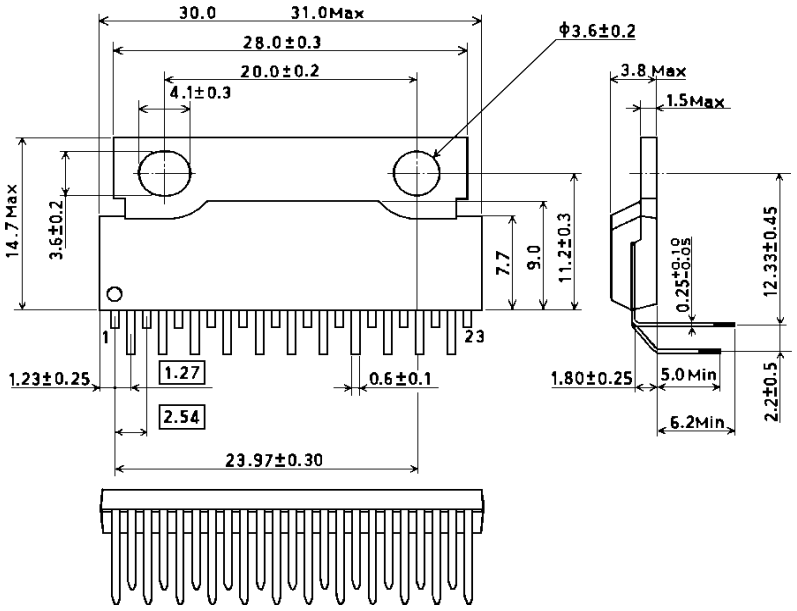


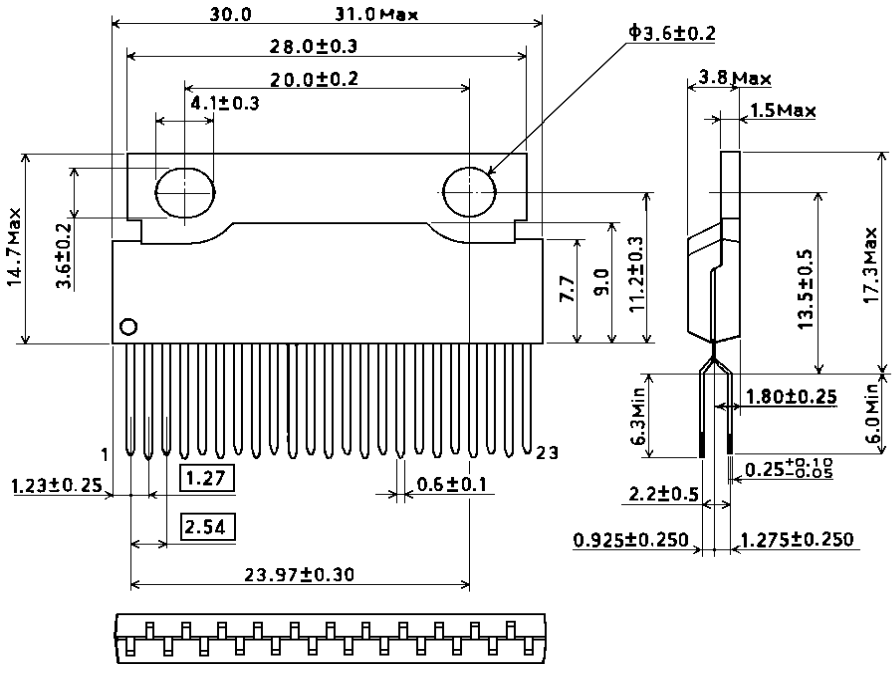
Figure 6. ECN3018 Safe Operating Area (SOA)

2. Package Dimensions

1) ECN3018SP



2) ECN3018SPV



3) ECN3018SPR