# ECN3067 APPLICATION NOTE

## 1. Introduction

ECN3067 is a one-chip three-phase bridge inverter IC that has 6 IGBTs in the circuit.

The IC is suitable for the speed control of three-phase induction motors and DC brushless motors applied to AC200-230V power supplies. It drives motors at up to 140W classes.

## 2. Internal block and its functions

Figure 1 shows the internal block diagram (with bootstrap system driven) and the functions.

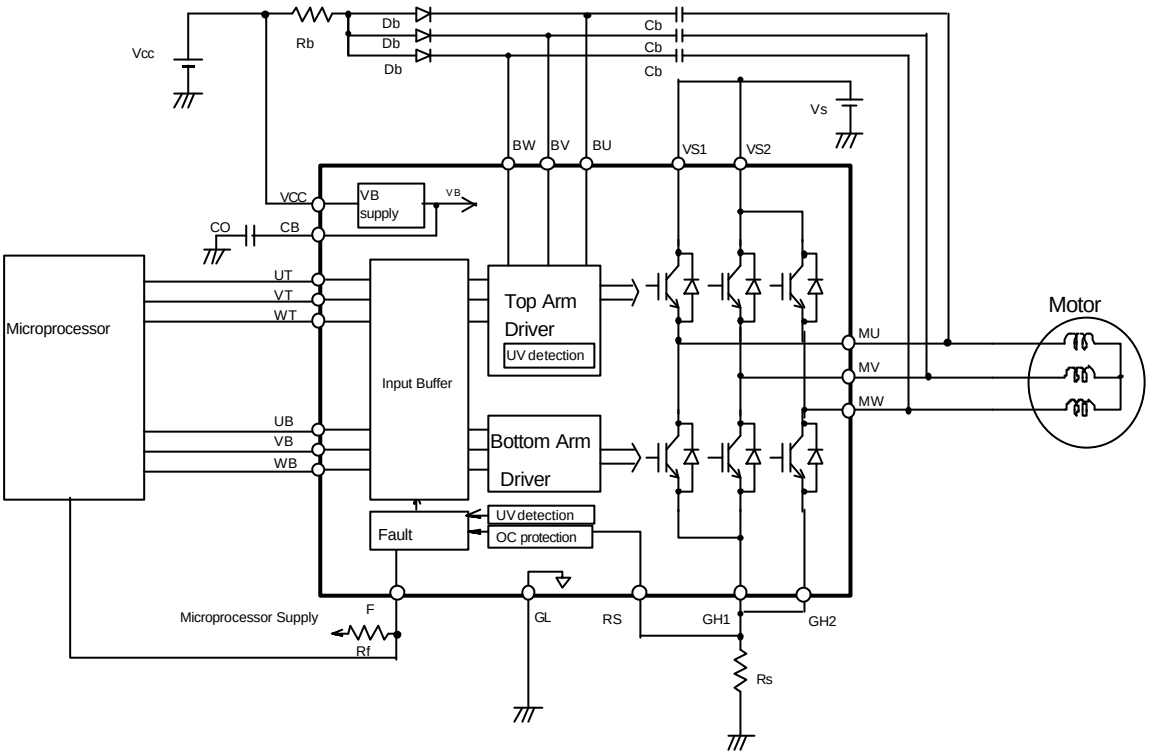



Fig. 1 Block Diagram (with bootstrap system driven)

### (1) Input Buffer

An ECN3067 package has a total of six input terminals; three top arm device inputs (marked with T) and three bottom arm device inputs (marked with B). UB, VB and WB are U, V and W phase inputs for the bottom arm devices, respectively. And UT, VT and WT are U, V and W phase inputs for the top, respectively.

Six input terminals are compatible with 5V-CMOS or LSTTL outputs.

Input of these terminals follows the negative logic and the output device, which connected with the input, is turned on when the input signal is low.

The terminals are pulled up by resistance Rp(200kΩ typ.) with internal supply VB=7.5V(typ.) in the internal circuit.

When ECN3067 is used connected to a microprocessor directly, a pull up resistance RH is needed for the six input terminals as shown in Figure 2 to avoid a breakdown and a latch up of output ports of a microprocessor.

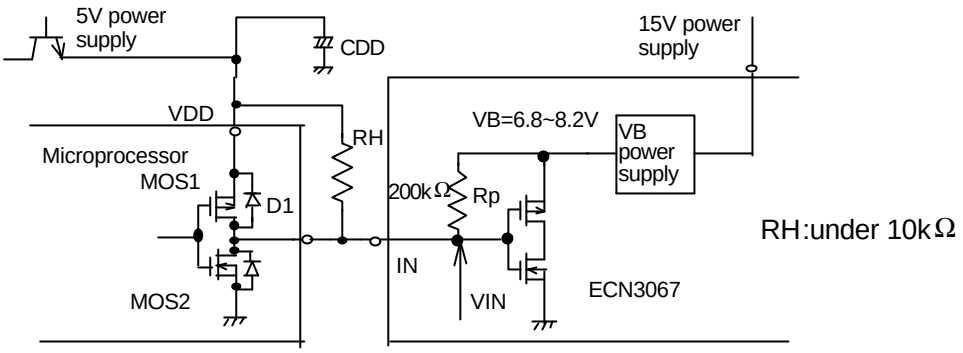



Fig.2 Example for pulling up in direct connection to microprocessor

**(2) Dead time**

The output device has a totem pole structure at IGBTs. If the top and the bottom IGBTs in the same phase are turned on simultaneously, the IC can be broken. A circuit for prevention against simultaneous turn-on is built in (See Truth Table in the Specification). The circuit, however, operates based on input time and does not consider the time gap caused by output delay. Accordingly, dead time has to be set up to allow the circuit to shift from the top (bottom) turn-off to the bottom (top) turn-on in the same phase without simultaneous on state. Figure 3 shows an example of dead time.

Shift from the top arm to the bottom in the same phase needs dead time longer than turn-off delay time for top arm (TdOFFT) and from the bottom to the top does turn-off delay time for bottom arm (TdOFFB). And, because the TdOFFT(TdON) characteristics depends on the temperature (See Fig.4), the dead time has to set up after consideration of the temperature dependence.

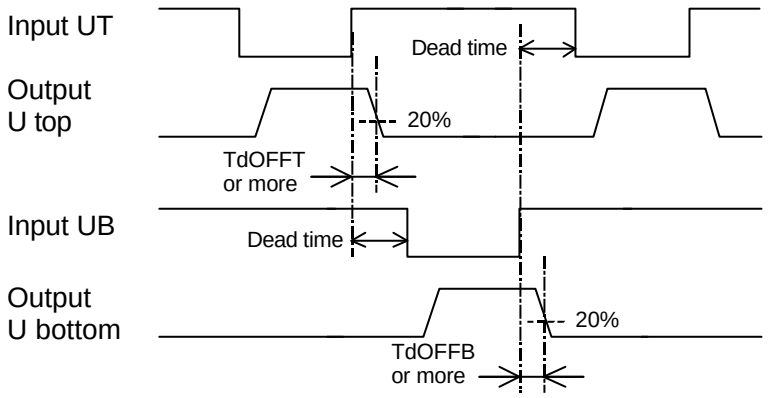



Fig. 3 Example of dead time set up

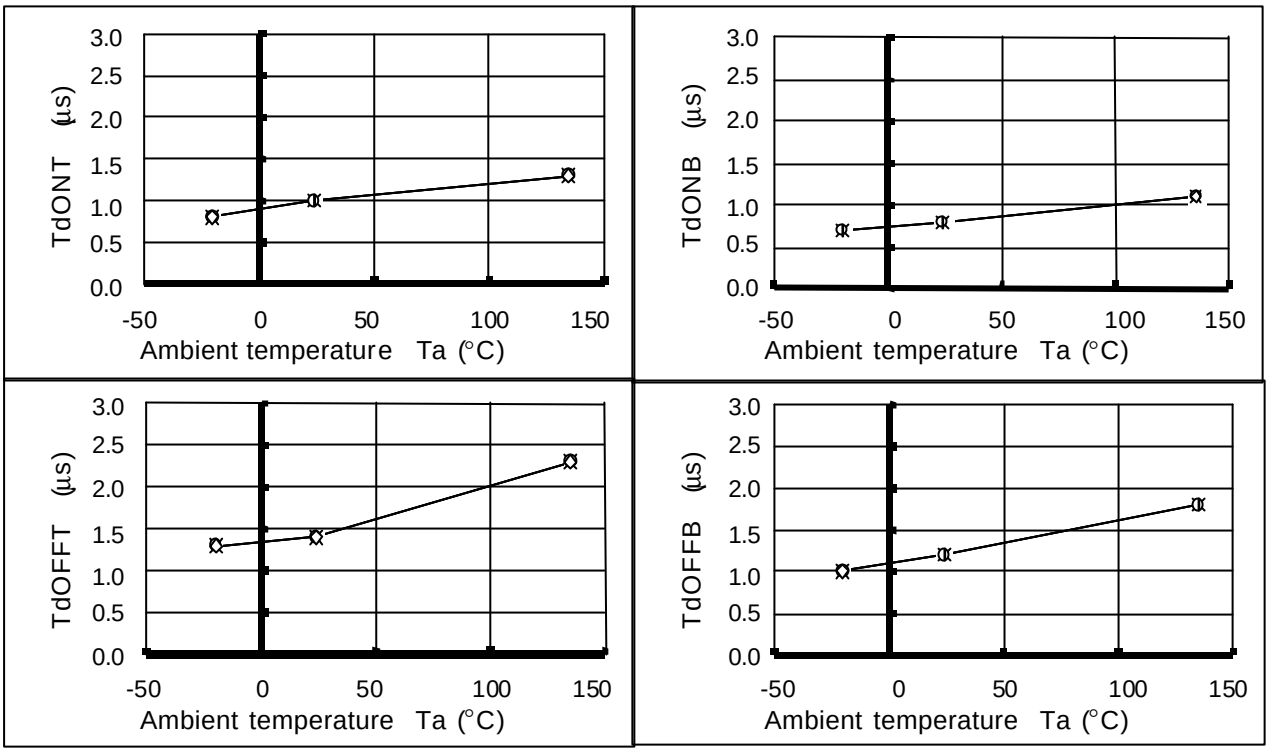



Fig. 4 Example of TdON / OFF temperature characteristics

**(3) Level shift circuit**

The top arm control circuit is operated under floating voltage indicated as [the output terminal potential + supply voltage Vcc]. The level shift circuit converts input signals at the ground level into top arm drive signals based on output voltage of each phase which constitutes floating potentials. A latch circuit inside the IC is triggered by edge of the top arm input signals, which reduces power consumption of the level shift circuit. (Refer to figure 5)

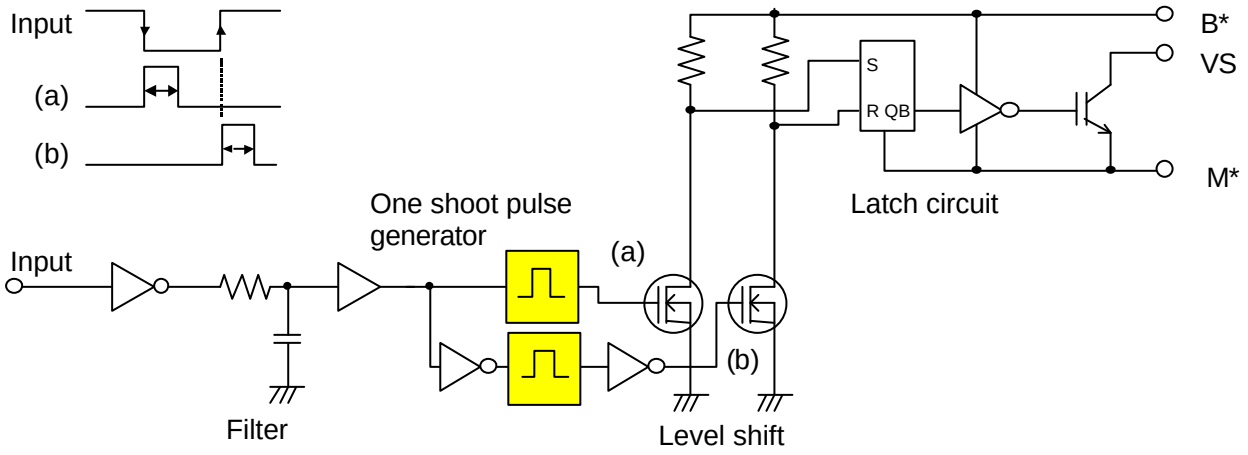



Fig. 5 Driver circuits organization of upper arm

**(4) Power supply of the top arm control circuit**

Each phase has two built-in IGBTs, which have a totem pole configuration. In order to turn on IGBTs, the gate voltage must be higher than the threshold voltage Vth (about 5V). In case of the bottom IGBTs, emitter of the IGBTs is fixed to the ground voltage; therefore, the gate voltage of the IGBTs is driven by the supply voltage Vcc.

In case of the top IGBTs, the gate voltage needs to be higher than the Vs voltage as the Emitter voltage of the IGBTs rises near to Vs. Floating power supply and bootstrap system are both applied for this operation.

**(a) Drive by floating power supply**

Figure 6 shows a circuit block diagram in drive by floating power supply.

Vfu, Vfv and Vfw in the figure indicate the three floating supplies.

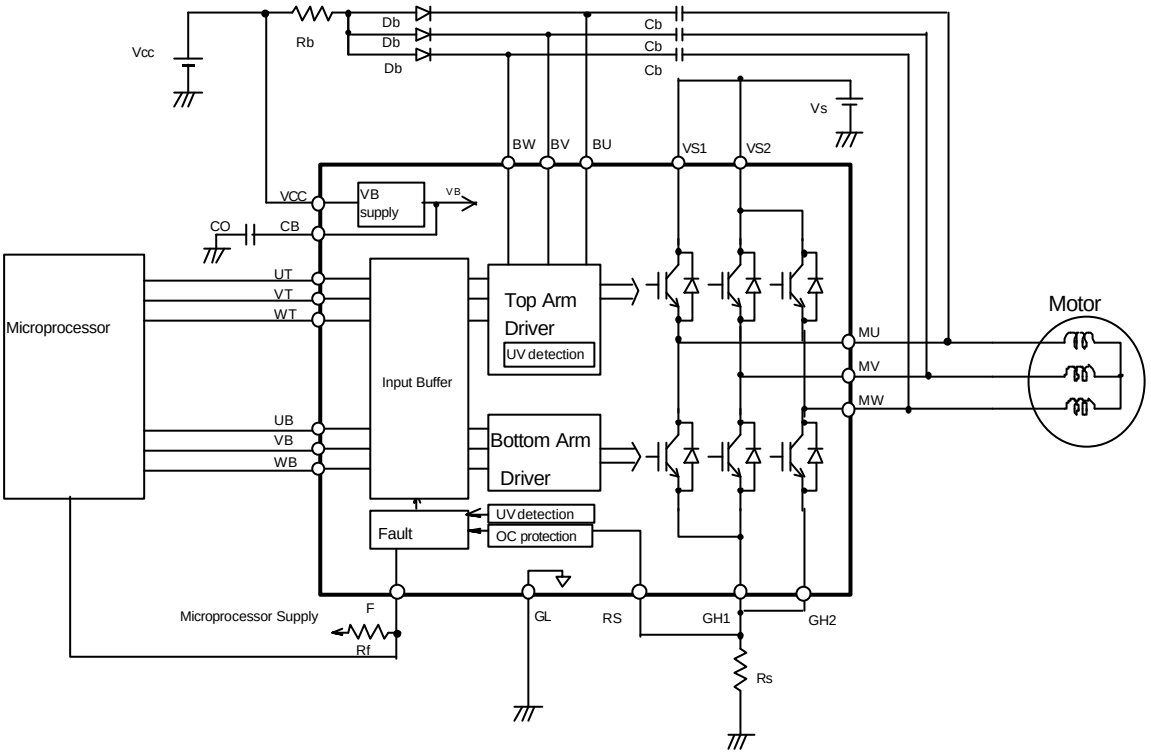



Fig.6 Circuit block diagram driven by floating power supply

**(b) Drive in bootstrap system**

Figure 1 shows drive in bootstrap system.

External capacitors marked with Cb are installed as power supply for the top arm driving circuit. One of the Cb terminals is connected to the Emitter of IGBTs to get the circuit higher voltage than Vs.

Vcc charges capacitor Cb through diode Db when the output terminal potential gets down to the ground level. There are two circumstances for the operation;

1. The bottom arms IGBTs are turned on.
2. The top arm IGBTs are turned on and the current consequently flows in the motor, and top arm IGBTs are turned off.

At the stand-by state, charge at Cb is regularly consumed by a stand-by current ISB(15μA typical) of the top arm control circuit. At that time, because bootstrap operation doesn't work, the top arm supply

voltage gets lower.

At the operation, the charge at Cb is also consumed by IGBT gate capacitor charge at the time of switching the top arm and switching the internal logic in the circuit. In these cases, because bootstrap operation works as stated above, the Cb is charged. The drop of the top arm supply voltage is not usually problem.

When bootstrap system is not on for a while, the top arm supply voltage gets lower. If the top arm supply voltage falls below the detection level, the top arm IGBTs are automatically turned off for the function of the under voltage protection. (Refer to Item No.4-(2) )Driving by bootstrap system costs less than by floating power supply, but the capacitor needs to be charged at the beginning to drive the top arm circuit. In addition, the Cb is influence on on-time duration of the top arm IGBTs. Attention should be paid especially when carrier frequency of pulse width modulation is low.

**(5) Functions**

**1) Bottom arm under voltage detection**

When Vcc falls below the under voltage detection level (11.4V typical) of the bottom arms, the protective circuit turns off the IGBTs of all the arms and sets the fault output terminal logic for "L" at the same time. The drop of Vcc voltage causes the drop of the gate voltage of the IGBT and IGBT sifts from linear area to saturation area and at last the IGBT destroy for the saturation.

The function of the under voltage protection prevents the IC from destruction.

**2) Over current protective function**

When the input voltage of RS terminal exceeds a specified value, Vref (0.5V typical), the protective circuit turns off the IGBTs of all the arms and sets the fault output logic for "L". The over current protection setting level (Io) is determined by the following equation;

Io = Vref / Rs (Rs is an external resistance)

A filter around about 0.4μs is equipped inside the RS terminal (See Figure 7). When over current protective function works by mistake due to some noises, external filter with R1 and C1 should be added. Take care not to allow delay of current sense signals; it can be happen when R1 and C1 are too large.

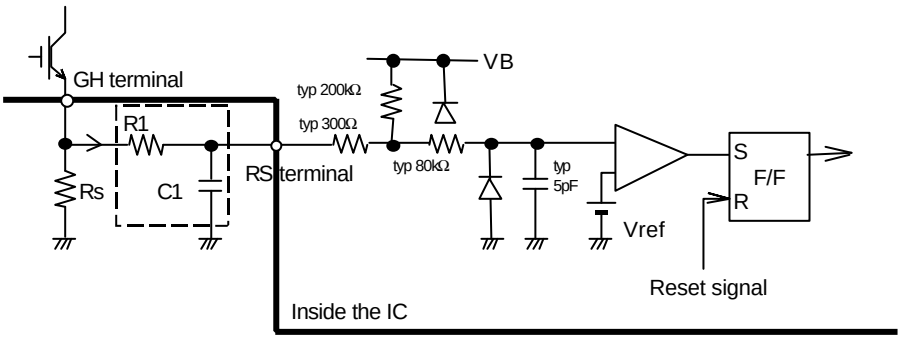



Fig. 7 Internal equivalent circuit of RS terminal

**3) Top arm under voltage protection**

When any of the potentials BU-MU, BV-MV or BW-MW falls below the under voltage detection level (11.4V typical). The protective circuit turns off the IGBTs of a top arm only in corresponding phase. The fault output remains unaffected in this case.

When the top arm IGBT turns off for this protective function, the top arm IGBT doesn't automatically

return even if the top arm supply voltage recover form the drop.

The IGBT doesn't turn on even if the input signal remains at the same state. Because of the latch function described at the level sift circuit (Item No.2-(3)), this state occurs.

In order to turn on in the top arm IGBT, the input signal once has to be turned from low to high and continuously has to be turned to low.

**4) Fault output terminal**

The terminal has an open-drain structure of N-MOS. Pull it up to CB or 5V via external resistance Rf (See Figure 8). Rf should be 5.6 kΩ or more.

A Photo coupler, if necessary, should be connected between CB and Fault as shown in Figure 9. The Fault output current is to be 5mA (typical) and limit resistance Rfc around 1kΩ be connected.

In order to reset a fault output, which has reached L-level, reset all the six input terminals of the top and the bottom for H-level. As for time delay of Fault reset, input "tflrs" or more here at this level. The reset can also be carried out by Vcc off and on (under voltage protective operation of the bottom arms).

Therefore, because of the limitation of the power supply sequence (refer Item No.4-(1)) , the reset of the Vcc isn't recommended.

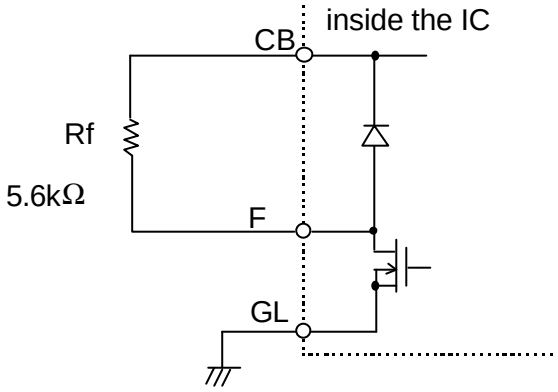



Fig. 8 Pull-up resistance installation

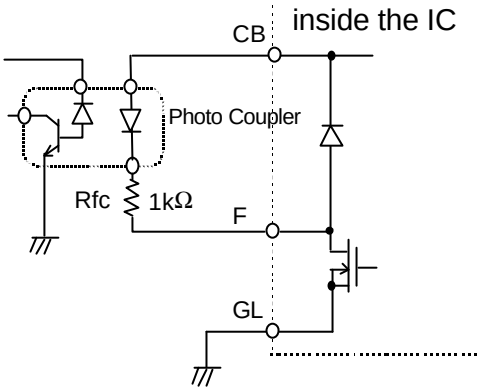



Fig. 9 Photo coupler installation

**5) VB power supply**

The input buffer, the bottom arm protective circuit, fault logic circuit and others operate with an internal power supply voltage VB=7.5V (typical) generated at Vcc supply.

CB terminal must be connected with an oscillation-preventive capacitor Co (0.22μF).

When external circuits and other are connected with the CB terminal. The capacitor Co added to stabilize the internal power supply had better set several μF. At the transient of the power supply sequence and so on, if Co is too large, delay time in operation of the internal power supply occurs, and miss-operation of the IC output rarely appears.

If you are obliged to add to too large Co, after well stabilization of the internal power supply you had better add the input signal.

VB output current has to use within the limit of the IB spec (50mA MIN.). If VB output current is too high, VB output voltage falls down. And there is a possibility that miss-operation of the internal logic circuits occur.

**3. Power consumption**

**(1) Summary**

ECN3067 series is roughly classified into three types of power consumption as below;

1) Power dissipation for forward drop IGBTs and free wheel diodes (steady-state dissipation)
2) Power dissipation for switching of IGBTs and free wheel diodes
3) Power dissipation inside the controlling circuit

Dissipation rates classified into 1) and 2) are in proportion to the value of output current.

**(2) Equations for calculating power consumption**

Power consumption mainly depends on the motor drive control system. Here are stated two ways of calculation of the value; 120° commutation controlled inverter system generally used for driving DC brushless motors and 180° sine wave commutation controlled inverter system used for driving induction motors.

**(a) Inverter controlled 120° commutation mode (bottom arm PWM chopping)**

**Total IC power consumption P = Pon + Pt + Pis + Picc** (W)

**Steady-state output dissipation Pon = $P_{IGT}$ + $P_{IGB}$ + $P_{DT}$** (W)

Top arm IGBTs dissipation $P_{IGT} = I \times V_{FT}$ (W)

Bottom arm IGBTs dissipation $P_{IGB} = I \times V_{FB} \times D$ (W)

Diode dissipation $P_{DT} = I \times V_{FDT} \times (1 - D)$ (W)

D : PWM duty

I : Motor RMS current (A) (See Fig.10)

$V_{FT}$ : Output device (IGBTs) FVD for Top arm (V)

$V_{FB}$ : Output device (IGBTs) FVD for Bottom arm (V)

$V_{FDT}$ : Diode FVD (V)

**Dissipation of output switching Pt = ( Eon + Eoff ) ´ fpwm**

Eon : Power/pulse generated in on-switching (J/pulse)

Eoff : Power/pulse generated in off-switching (J/pulse)

fpwm : PWM frequency (Hz)

**Vs supply power consumption (on stand-by) Pis = Vs ´ Is » 0 (W)**

**Vcc supply power consumption (on stand-by) Picc = Vcc ´ Icc » 0.11 (W)**

Vs : Vs supply voltage (V)

Vcc : Vcc supply voltage (V)

Is : Vs supply current (A)

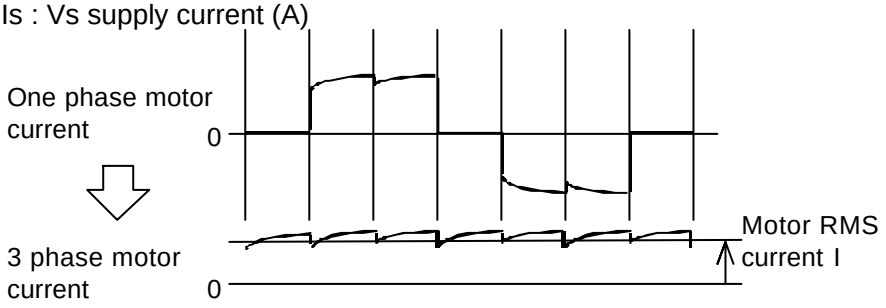



Fig. 10 Definition of motor RMS current I

**(b) Inverter controlled 180° sine wave commutation mode (all arms PWM chopping)**

**Total IC power consumption P**

**= P(sat)AV + P(fwd)AV + P(SW)AV + P(R)AV + Pis + Picc**

**IGBT steady-state dissipation P(sat)AV = Ip ´ $V_{FB}$ ´ (1 / 8 + D / (3 π) ´ cos θ) ´ 6 (W)**

**Diode steady-state dissipation P(fwd)AV = Ip ´ $V_{FD}$ ´ (1 / 8 - D / (3 π) ´ cos θ) ´ 6 (W)**

**IGBT recovery dissipation P(SW)AV = $E_{SW}$ ´ fpwm/π ´ 6 (W)**

**Diode recovery dissipation P(R)AV =1 / 8 ´ (Irr ´ Vs ´ trr ´ f) ´ 6 (W)**

**Vs supply power consumption (on stand-by) Pis = Vs ´ Is » 0 (W)**

**Vcc supply power consumption (on stand-by) Picc = Vcc ´ Icc » 0.11 (W)**

Ip : Peak current (A) (See Fig.11)

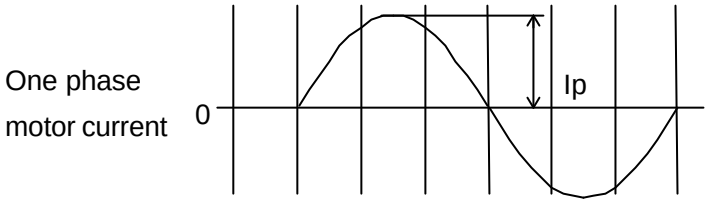
Esw : Esw = Eon + Eoff Power/pulse generated in switching (J/pulse)

cosθ : Power factor D : PWM duty fpwm : PWM frequency (Hz)

trr : Diode recovery time (s) Irr : Diode recovery current (A)

Vs : Vs supply voltage (V) Is : Vs supply current (A)

Vcc : Vcc supply voltage (V) Icc : Vcc (A)




Motor RMS current I = Ip / $\sqrt{2}$

Fig. 11 Definition of Motor RMS current I

### (3) Example for calculating power consumption

#### (a) Inverter controlled 120° commutation mode (bottom arm PWM chopping)

Figure 12 shows an example of calculation of power consumption rate. Refer to Chart 1 for its conditions. Data on Eon and Eoff will be shown in Figure 14 and 15.

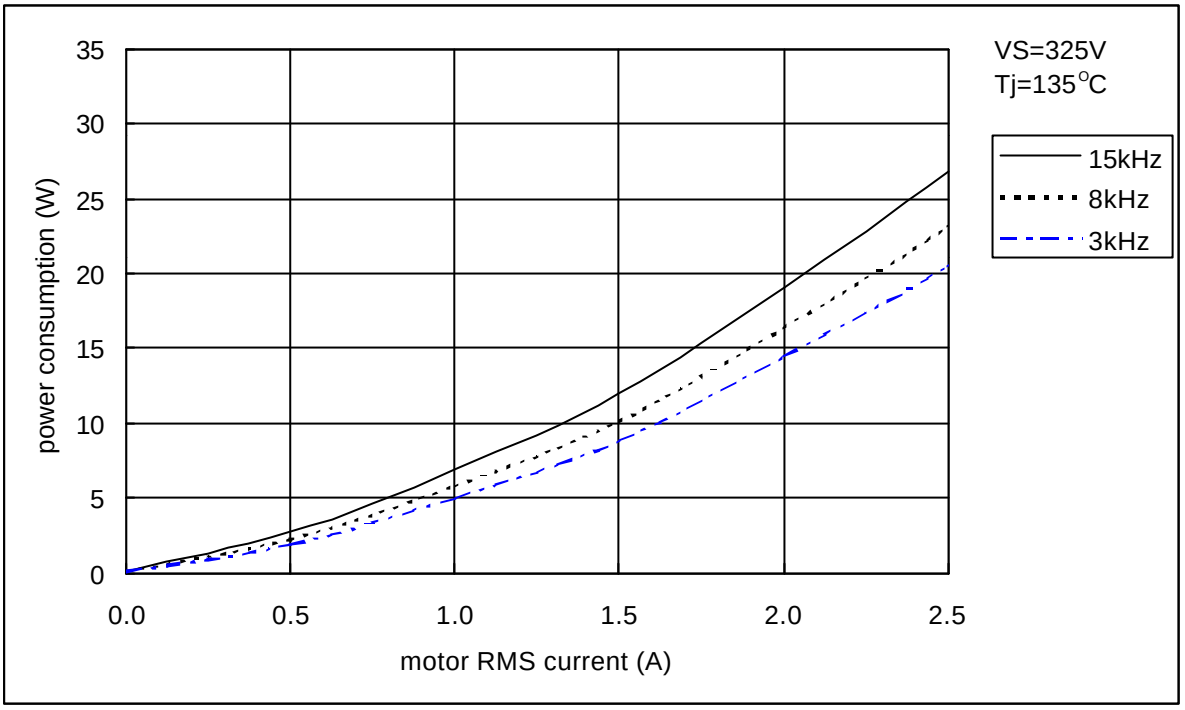



Fig. 12 Example of 120° commutation mode (bottom arm PWM chopping)

Chart 1 Calculating conditions for 120° commutation mode

| No. | Item | | Symbol | Motor RMS Current(A) | | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|
| | | | | 0.5 | 1.0 | 1.5 | | |
| 1 | VS Supply Voltage | | Vs | 325 | 325 | 325 | V | |
| 2 | Output Current | | I | 0.50 | 1.00 | 1.50 | A | |
| 3 | Junction Temperature | | Tj | 135 | 135 | 135 | °C | |
| 4 | Output device FVD | Top arm IGBTs | VFT | 1.6 | 2.3 | 2.7 | V | 135°C |
| | | Bottom arm IGBTs | VFB | | | | | |
| 5 | Diode FVD | | VFD | 1.5 | 1.8 | 2.3 | V | 135°C |
| 6 | PWM Frequency | | fpwm | 3.0 | 3.0 | 3.0 | kHz | |
| 7 | PWM duty | | D | 0.7 | 0.7 | 0.7 | - | |
| 8 | Power/Pulse generated in On -Switching | | Eon | 0.025 | 0.067 | 0.126 | mJ/pulse | 325V,135°C |
| 9 | Power/Pulse generated in Off –Switching | | Eoff | 0.044 | 0.089 | 0.136 | mJ/pulse | 325V,135°C |
| 10 | VS Standby Current | | Is | 0.0 | 0.0 | 0.0 | mA | |
| 11 | Vcc Standby Current | | Icc | 7.0 | 7.0 | 7.0 | mA | |
| 12 | Top arm IGBTs Dissipation | | PIGT | 0.80 | 2.30 | 4.05 | W | |
| 13 | Bottom arm IGBTs Dissipation | | PIGB | 0.56 | 1.61 | 2.84 | W | |
| 14 | Diode Dissipation | | PDT | 0.23 | 0.54 | 1.04 | W | |
| 15 | Dissipation of switching | | Pt | 0.21 | 0.47 | 0.79 | W | (Eon+Eoff)× Fpwm |
| 16 | VS Supply Power Consumption | | Pis | 0.00 | 0.00 | 0.00 | W | |
| 17 | VCC Supply Power Consumption | | Picc | 0.11 | 0.11 | 0.11 | W | |
| 18 | Total IC Power Consumption | | P | 1.91 | 5.03 | 8.83 | W | |

**(b) Inverter controlled 180° sine wave commutation mode (all arms PWM chopping)**

Figure 13 shows an example of calculation of power consumption rate. Refer to Chart 2 for its conditions. Data on Eon and Eoff will be shown in Figure 14 and 15.

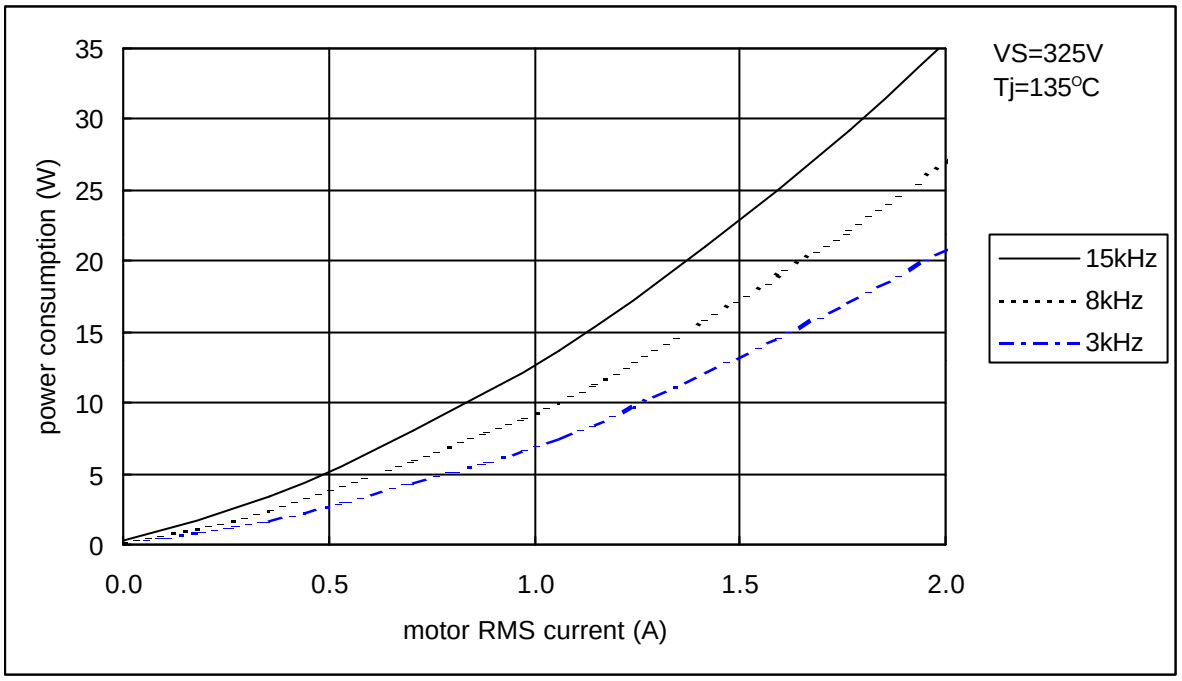



Fig. 13 180° sine wave commutation mode (all arms PWM chopping)

Chart 2 Calculating conditions for 180° sine wave commutation mode

| No. | Item | | Symbol | Motor RMS Current(A) | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|
| | | | | 0.4 | 0.7 | 1.1 | | |
| 1 | VS Supply Voltage | | Vs | 325 | 325 | 325 | V | |
| 2 | Output Current | | Ip | 0.50 | 1.00 | 1.50 | A | |
| 3 | Junction Temperature | | Tj | 135 | 135 | 135 | °C | |
| 4 | Power Factor | | cosθ | 0.95 | 0.95 | 0.95 | - | |
| 5 | Output device FVD | Top arm IGBTs | VFT | 1.6 | 2.3 | 2.7 | V | 135°C |
| | | Bottom arm IGBTs | VFB | | | | | |
| 6 | Diode FVD | | VFD | 1.5 | 1.8 | 2.3 | V | 135°C |
| 7 | Diode Recovery Current | | Irr | 0.3 | 0.3 | 0.3 | A | |
| 8 | Diode Recovery Time | | trr | 0.15 | 0.15 | 0.15 | μs | |
| 9 | PWM Frequency | | fpwm | 3.0 | 3.0 | 3.0 | kHz | |
| 10 | PWM duty | | D | 0.7 | 0.7 | 0.7 | - | |
| 11 | Power/Pulse generated in On -Switching | | Eon | 0.025 | 0.067 | 0.126 | mJ/pulse | 325V,135°C |
| 12 | Power/Pulse generated in Off –Switching | | Eoff | 0.044 | 0.089 | 0.136 | mJ/pulse | 325V,135°C |
| 13 | VS Standby Current | | Is | 0.0 | 0.0 | 0.0 | mA | |
| 14 | Vcc Standby Current | | Icc | 7.0 | 7.0 | 7.0 | mA | |
| 15 | Steady-state Dissipation | Top arm IGBTs | P(sat)AV | 0.94 | 2.70 | 4.75 | W | |
| 16 | Steady-state Dissipation | Bottom arm IGBTs | P(fwd)AV | 0.25 | 0.59 | 1.13 | W | |
| 17 | Diode Steady-state Dissipation | | P(SW)AV | 0.40 | 0.90 | 1.50 | W | |
| 18 | Diode Recovery Dissipation | | P(R)AV | 0.03 | 0.03 | 0.03 | W | |
| 19 | VS Supply Power Consumption | | Pis | 0.00 | 0.00 | 0.00 | W | |
| 20 | VCC Supply Power Consumption | | Picc | 0.11 | 0.11 | 0.11 | W | |
| 21 | Total IC Power Consumption | | P | 1.72 | 4.32 | 7.52 | W | |

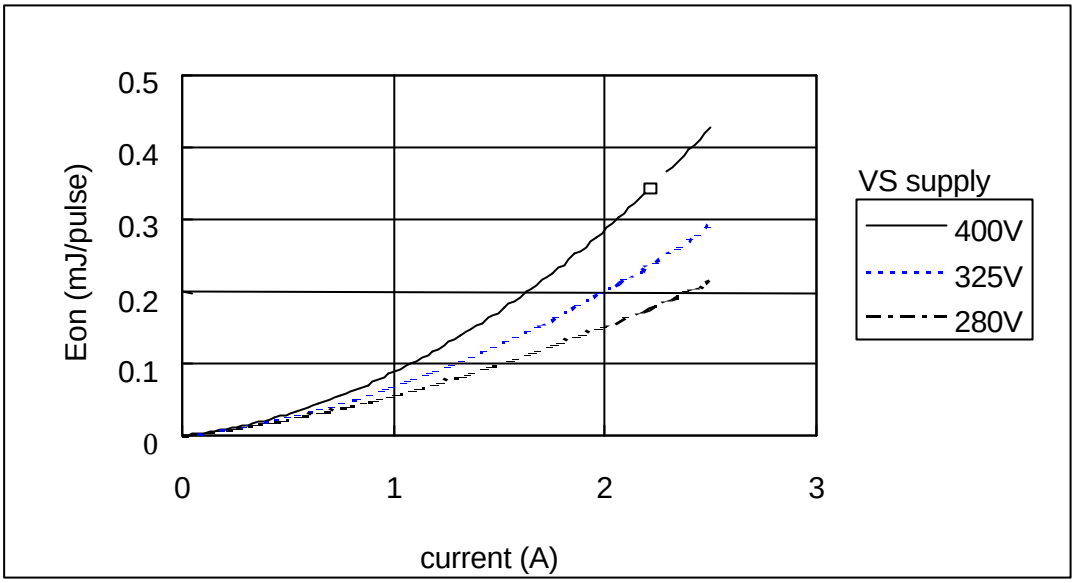



Fig. 14 Eon measurement data

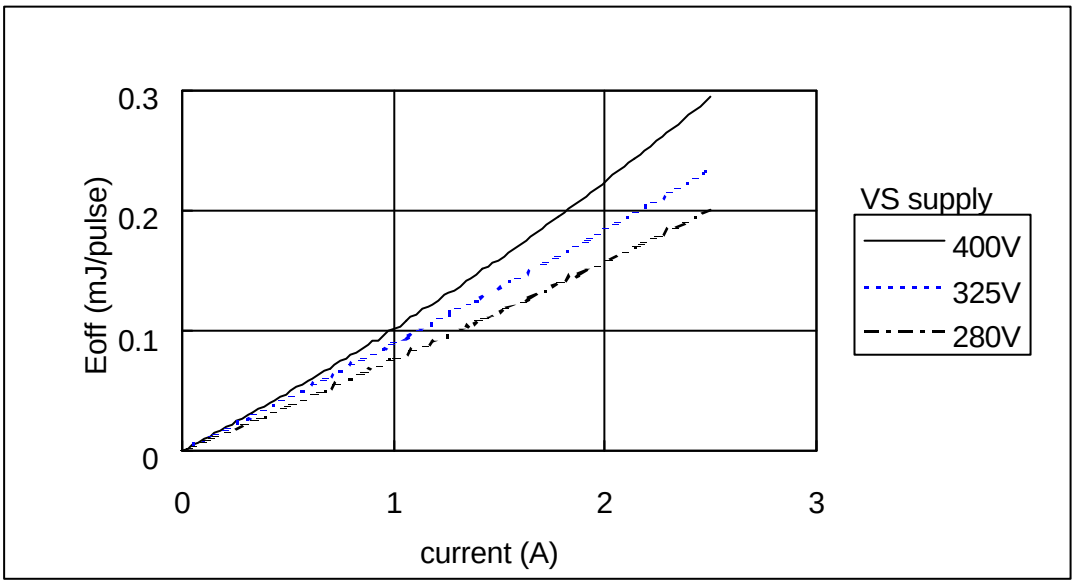



Fig. 15 Eoff measurement data

**(4) Maximum allowable case temperature**

The followings are examples of calculations of the maximum allowable case temperature under two different conditions.

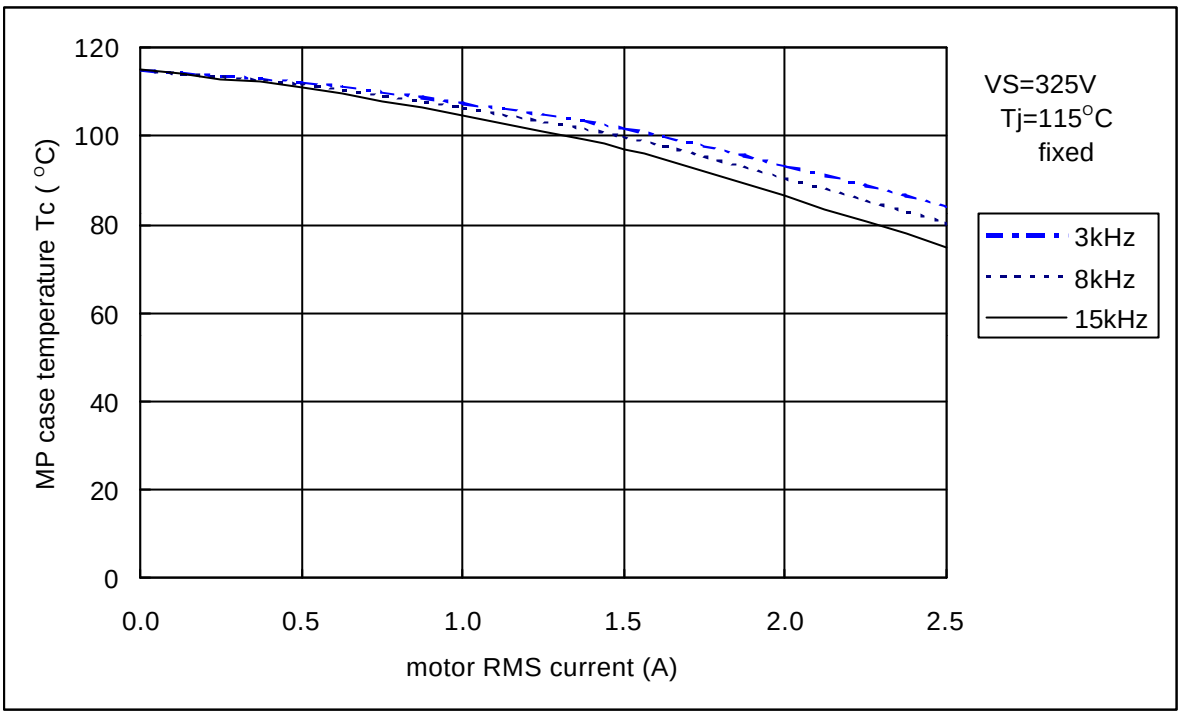



Fig. 16 Maximum allowable case temperature (120° Tj=115°C fixed)

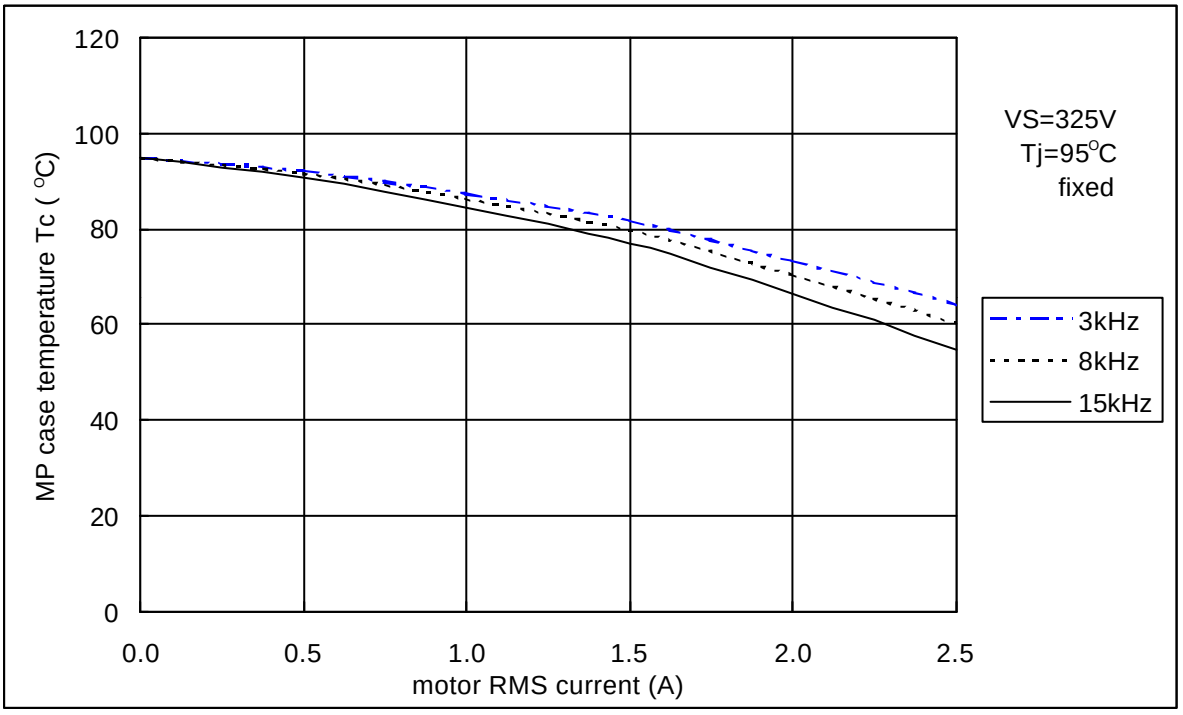



Fig. 17 Maximum allowable case temperature (120° Tj=95°C fixed)

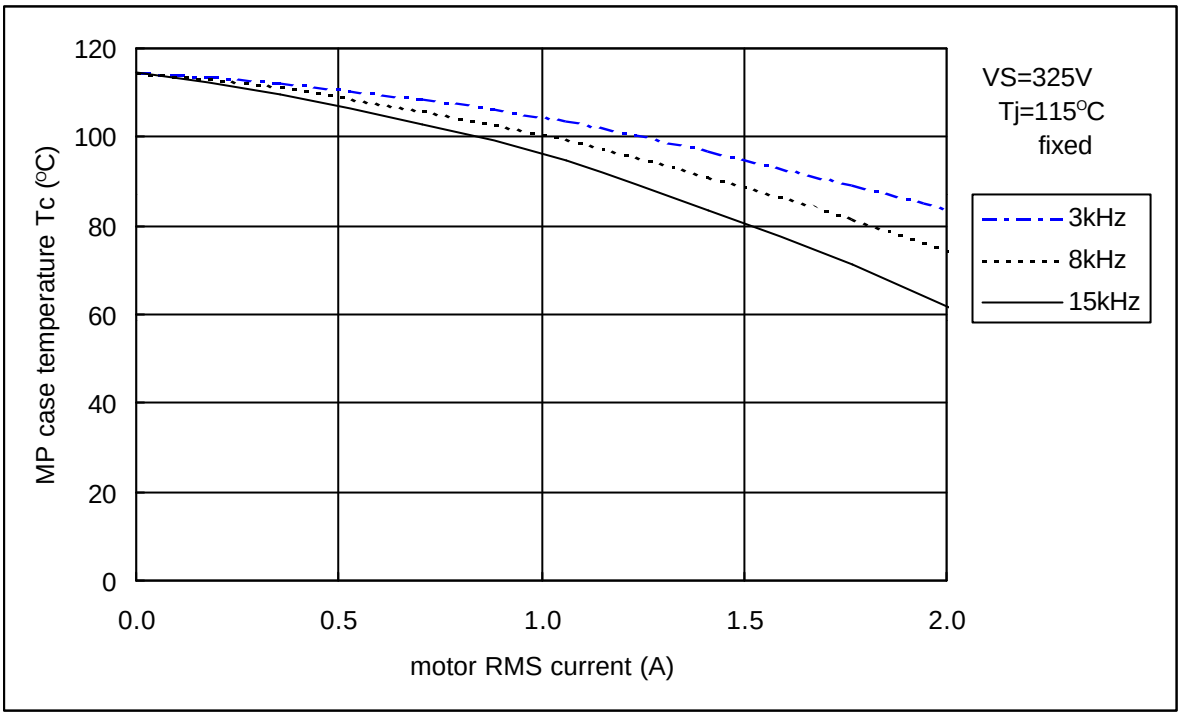



Fig. 18 Maximum allowable case temperature (180° Tj=115°C fixed)

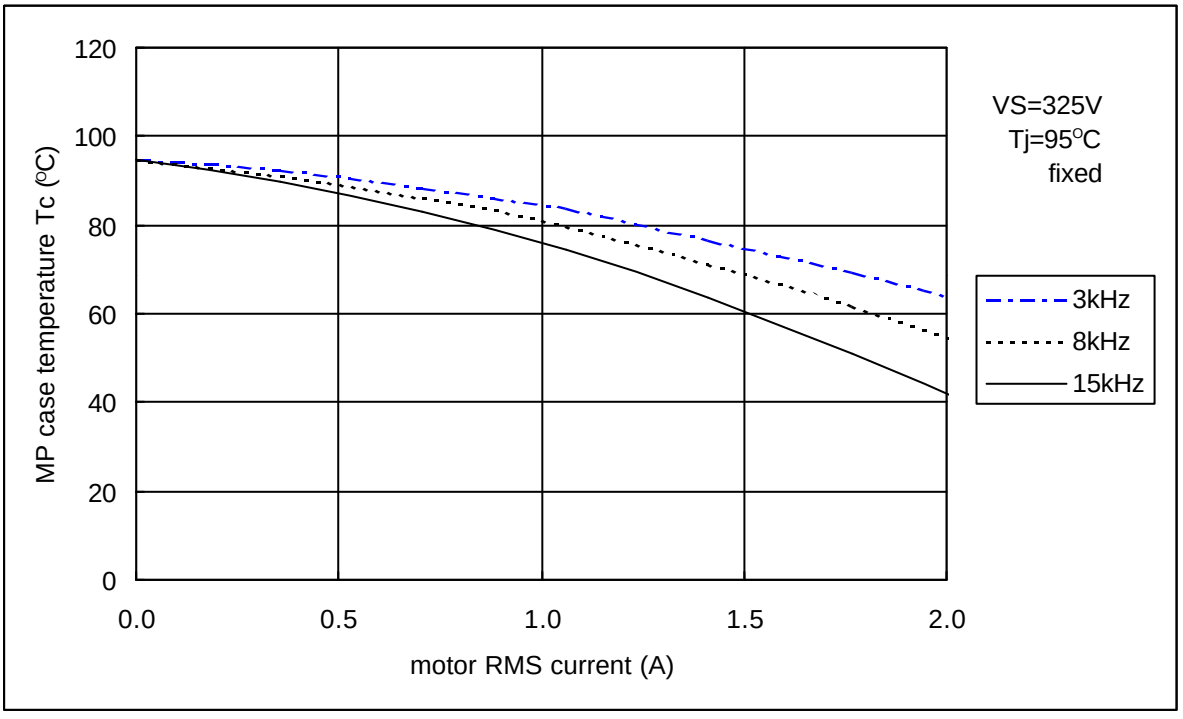



Fig. 19 Maximum allowable case temperature (180° Tj=95°C fixed)

**(5) Thermal radiation**

Thermal resistance Rth(c-a) of a heat spreading fin is calculated as follows;

Rth(c-a) = ( Tcmax – Ta ) / P (°C /W)

Ta : Ambient temperature, Tcmax : Maximum allowable case temperature

P : Power consumption

Set conditions 120° commutation mode, fpwm=3kHz and output current I=1A as a case.

Power consumption is worked out at around 5W on Figure 12 and the maximum allowable temperature at 90°C on Figure 17. Here set Ta=60°C, thermal resistance of a heat spreading fin is calculated by the equation above;

( 90 – 60 ) / 5 = 6 °C /W

## 4. Instructions

**(1) Power supply sequence**

Turn-on and turn-off of the output IGBT are controlled by the gate voltage. In case of the bottom arm IGBT, the gate voltage is the Vcc supply voltage (between Vcc and GND). On the other hand, in the top arm IGBT, the gate voltage is the BU, BV and BW-terminal voltage (between BU and MU, between BV and MV, and between BW-MW).

Fig.20 indicates the output characteristic of the IGBT. VG is the gate voltage. In this figure, as the voltage between collector and emitter of the IGBT (Vce) is close to 10 volt , collector current (Ic) is slowly hand to flow. And the Vce more increase, the IC shows a characteristic of a constant current. The state of the characteristic is called saturation state. When the IGBT goes to the saturation states, power consumption increase and a temperature suddenly rise. When the IC's junction temperature exceeds a specified value, Tjop (135°C), there is a possibility of the IC destroying.

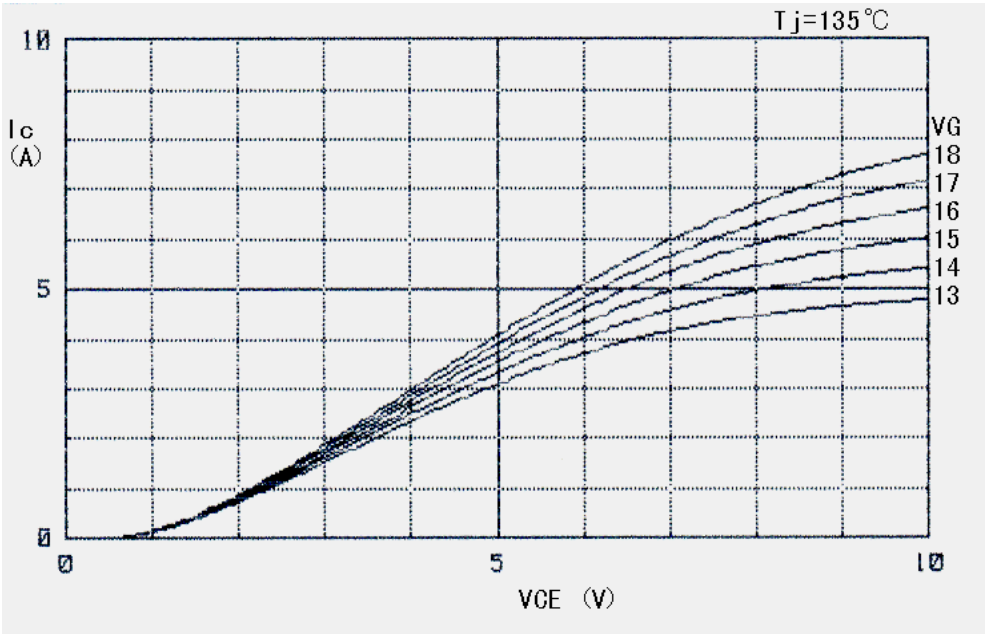



Fig. 20 Example of IGBTs output characteristics

In the power sequence, from the minimum figure (13.5V) of the VCC Recommended Operating Conditions to the minimum figure (9.8V) of the under detective voltage, there is a possibility the low gate voltage driving the IGBT.

For example, when the motor start to operate after the Vcc is applied last, the IGBT is easy to be saturation state and there is a possibility of the IC destroying.

And when the motor is stopped, if the Vcc is fallen down before, the IGBT is easy to be saturation state as like above case.

Therefore, due to the control of the speed for the rise and / or fall of the Vcc the IGBT's fever can be suppressed. But the speed has to be the several micro second.

Accordingly, the power sequence is the following. The input should be controlled at the stabilization of the Vcc. Vs is passed over.

**(2) Bootstrap capacitor Cb, diode Db and current limiting resistance Rb**

On-duration of the top arm IGBTs can lead discharge of capacitor Cb in the top arm circuit current, which accordingly lowers supply voltage and operates the top arms under voltage protection. Time period for supply voltage to decrease ($\tau$) is roughly indicated as below;

$\tau = ( Cb \times VBU / ISB \times Ln ( VBU / Vuvt )) \quad (s)$

VBU : top arm supply voltage ISB : top arm standby current

Vuvt : top arm under voltage protective operation level

Ln : natural logarithms

Calculation in the case of Cb=3.3μF is;

$\tau = ( 3.3\mu F \times 15V / 15\mu A \times Ln ( 15V / 11.4V ))$

$= 0.9 (s)$

Here the maximum on time of the top arm IGBTs is 0.9s.

At the above case, on-time is calculated using the under voltage detective level (Vuvt). But the IGBT saturation state at the power sequence which described In the Item No. (1), has to be considered. Accordingly, it is the best that the minimum figure (13.5V) of the Vcc recommended operating conditions is used in the above calculation as a figure of the Vuvt. Result of the calculation is that the on-time is equal to approx. 0.3s. In this case, after the bootstrap operation stop, the top-arm IGBT has to be turned-off within 0.3s.

Connect Cb in the closest position to the IC to avoid its fatal damage by excess voltage.

Current limiting resistance Rb controls the maximum value of charged current in Cb under the permissible value of the surge current in diode Db as well as prevents over current protection from operation at initial charge.

Rb is decided from below equation at a rough estimate.

$ibpeak = Vref / Rs$

$Rb > ( Vcc \times Rs ) / Vref \times 2 \quad ( \times 2 : margin )$

ibpeak : peak current of a initial voltage charge

Rs : shunt resistance

Vref : Over current reference voltage

Above argument is considering for one phase, but in actual system the initial voltage charge must be considered for three phase. Because of motor, which is connected to IC, make short cut circuit between three Cb capacitor.

After all, ibpeak must be estimated as three times as above calculation.

If the period of charging time will be too long, it is acceptable to use Rb resistance series to Db diode for each phase.

Characteristics of diode Db should be characterized by breakdown voltage of more than 500V forward voltage small enough and reverse recovery time trr under 200ns.

Recommended devices;

Db : HITACHI DFG1C6 or DFM1F6

[600V/1A, Trr ≤ 100ns]

Cb : 3.3μF [Stress voltage = Vcc]

**(3) Initial input set up for bootstrap capacitor charging**

When bootstrap system is introduced as a driver of top arm control circuit, the bootstrap capacitor needs to be charged with 11V or more so that the top arm IGBTs get turned on. The initial charge, therefore, is required when the capacitor is zero V.

Cb will be charged by turn on the bottom arm of the corresponding phase. Turn on the power supply and then input pulses or on-signal for more than several ms as an initial set up.

**(4) Rs shunt resistance**

A shunt resistance which decided an over current protection level, and the wiring system have not to cause an inductance component to the utmost. The shunt resistance may generate negative surge voltage from this L-component (Ls) and di/dt under operation of over current protection.

The held current in Ls flows below path (Fig.21). The current flows from the GL-terminal, through the IC internal circuits and into the GH-terminal. This current may cause a destruction of IC and fever through the miss-turned-on of IGBT. In this case, make the surge voltage between GH-HL enough not to be beyond minus 5V. Method of effective suppression of the surge voltage is the following.

[1] Wiring of the shunt resistance system is shortened as much as possible.

[2] Non-inductive shunt resistance should be used.

[3] Set a diode (Ds) parallel to the shunt resistance, and a surge voltage is clamped. In this case, be careful that an effect of the diode differs at the difference of the connection point. Fast recovery diode is recommended as a Ds. (1A,breakdown voltage of 20V or more )

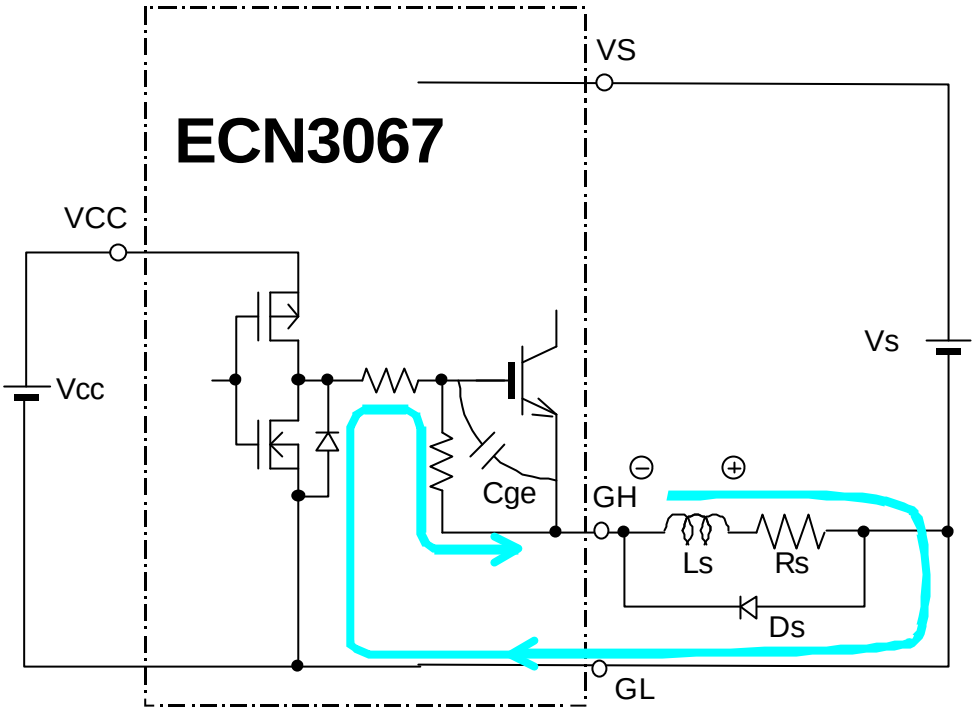



Fig. 21 Cause of over voltage generation at shunt resistance

**(5) GH1 and GH2 terminals**

These are connected to the emitters of the bottom arm IGBTs. Over-current can be detected by comparing the voltage drop, which is produced at a shunt resistance RS with Vref. GH1 should be connected to GH2 near IC pins.

**(6) Tabs**

Tabs, heat sinks of the IC itself, are not insulated from the IC. Attach an insulating sheet at low thermal resistance, if needed, when a chassis is to be used as an external heat sink and if it is needed to be insulated.

An independent external fin can be equipped without an insulating sheet. Tabs are as well at the ground potential of the IC in that case.

**(7) Power supply capacitor between VCC and GL**

Transient current at the peak of several 10mA flows in the internal logic circuit depending on output on/off with input signals and another transient current that charges bootstrap capacitor flows as well. Noise voltage indicated as [L×di/dt] caused at the VCC terminal of the IC by these currents and the wiring inductance may exceed the maximum allowable voltage and destroy devices. Please connect a capacitor (Cvc) to the IC as close as possible and see to it that the IC would not be overcharged when VCC terminal is not wired to the power supply close enough. (Fig.22)

Recommended capacitance of cue is more the free tone as bootstrap capacitor; Cb.

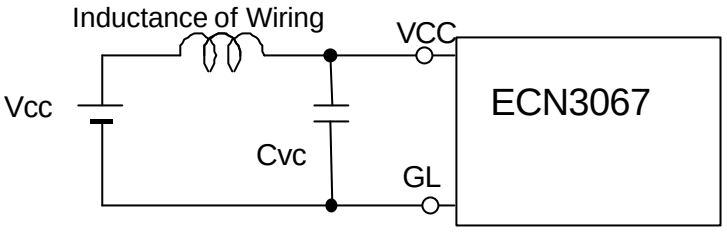



Fig. 22 Capacitance position in wiring system

**(8) Pin to pin insulation**

High voltage is applied between the following pins;

No.1-2 No.2-3 No.3-4 No.4-5 No.5-6

No.17-18 No.18-19 No.22-23

Applying molding or coating by resin and such to the pins in the IC is recommended. There are many kinds of resins, those thermal and mechanical stress on semiconductor devices, when put on, is yet unknown under influence of size and thickness of a base plate and such. Please make inquires to a circuit board manufacturer in selecting a resin for coating.

**(9) Breakdown by surge voltage**

When surge voltage is applied to VS terminal, the IC is possibly broken. The followings are effective in that case;

1) Install elements such as Zener diodes, which absorb surge voltage near to VS terminal.

2) Install a pass capacitor near to VS terminal. One with bigger capacity is more effective. Please apply a ceramic capacitor of at least 0.1μF.

**(10) Motor lock operation**

Over current detection continuously works when a certain top arm and a bottom arm IGBT are locked on state by motor lock. The IC junction temperature, then, exceeds Tjmax for the generated high power. ECN3067 does not have a protective function against motor lock operation. Take care not to leave the IC in that operation for a long time; it has a possibility to be broken.

**(11) Output short circuit protection**

Output short circuit protective functions against load short, line-to-ground short or the top and the bottom arm short are not built in. An output short circuit can cause the IC a damage.

**(12) Noise caution for input terminal**

Six input terminals UT, VT, WT, UB, VB, WB are sensitive and easily influenced by switching noise signal, due to the high input impedance.

Design of print circuit board must be avoid the noise signal to the six input terminals.

Using input terminal filter as shown fig.23, input signal from microprocessor would be delay to IC.

Check not occurring top and bottom IGBTs in same phase are turned on simultaneously, because of the delay.

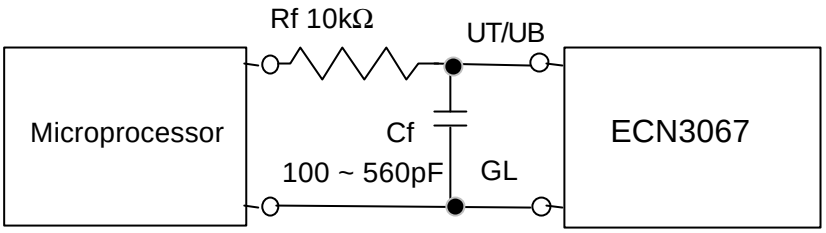



Fig. 23 Example of input terminal filter

**(13) Others**

Refer to “Instruction for Hitachi high voltage IC” for more information.

# HITACHI POWER SEMICONDUCTORS

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