
3-phase IGBT/MOS Gate Driver IC

ECN30552S Product Specification

Rev. 0

1. Product Description

1.1 Features

- (1) PWM control of top and bottom arms is possible with six control signals
- (2) Free run condition is detected by the built-in back EMF* detection circuit
- (3) Maximum Ratings: 620V, suitable for the system from 200VAC to 240VAC
- (4) Drives a motor using a high voltage DC power supply and a low voltage DC power supply (15V)

1.2 Functions

- (1) Six input type
- (2) FU and FV signal output pins for U and V-phase back EMF detection
- (3) Fault output pin
- (4) Built-in bootstrap diode
- (5) 5V power supply
- (6) Over-current protection function
- (7) Vcc low-voltage detection function
- (8) Top arm low-voltage detection function

*EMF: Electromotive Force

1.3 Block Diagram

FIGURE 1.3.1 shows block diagram.

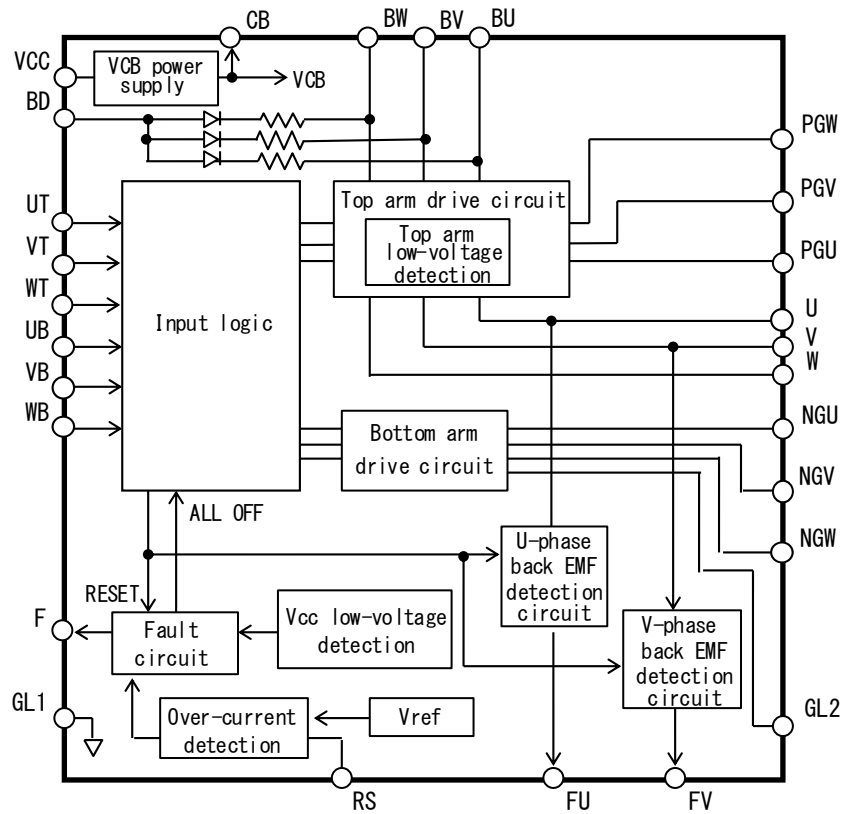
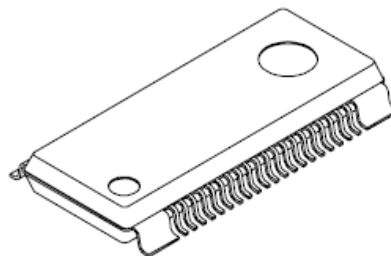


FIGURE 1.3.1 Block Diagram

1.4 Package



(Type of package: HSOP-36AN)

FIGURE 1.4.1 Package of ECN30552S

2. Specification

2.1 Maximum ratings

TABLE 2.1.1 Maximum ratings

Condition: Ta=25°C

| No. | Item | Symbol | Pin | Rating | Unit | Condition |
|-----|---------------------------------------|----------------------|-----------------------------|-----------------|------|--------------------------|
| 1 | High voltage device withstand voltage | VBV | BU,BV,BW | 620 | V | |
| 2 | GL2 pin voltage | VGL2 | GL2 | -5 to VCC | V | |
| 3 | U, V, W pin voltage | VU,VV,VW | U,V,W | -5 to 600 | V | |
| 4 | Voltage between BU-BD, BV-BD, BW-BD | VBUD VBVD VBWD | BU,BV,BW, BD | -5 to 600 | V | |
| 5 | Vcc power supply voltage | VCC | VCC,BD | 20 | V | |
| 6 | Voltage between BU-U, BV-V, BW-W | VBSU VBSV VBSW | BU,U BV,V BW,W | 20 | V | |
| 7 | Voltage between VCC-GL2 | VCCGL2 | VCC,GL2 | 23 | V | $-5V \leq VGL2 \leq -3V$ |
| 8 | Input voltage | VIN | UT,VT,WT UB,VB,WB, RS | -0.5 to VCB+0.5 | V | |
| 9 | Fault output voltage | Vflt | F | -0.5 to VCB+0.5 | V | |
| 10 | FU, FV output voltage | VFU,VFV | FU,FV | -0.5 to VCB+0.5 | V | |
| 11 | VCB supply output current | ICBMAX | CB | 50 | mA | |
| 12 | Junction operating temperature | Tjop | — | -40 to +125 | °C | |
| 13 | Storage temperature | Tstg | — | -40 to +150 | °C | |

Note 1: Thermal resistance

Between junction and case : Rjc = 3°C/W (Reference value)

2.2 Electrical Characteristics

TABLE 2.2.1 Electrical Characteristics (1/2) Suffix (T: Top arm, B: Bottom arm) Condition: Ta=25°C

| No. | Item | | Symbol | Pin | Min. | Typ. | Max. | Unit | Condition |
|-----|---|----------|--------|--------------------------------|------|------|------|------|---|
| 1 | Standby current | | Is1 | VCC | — | 3 | 10 | mA | VCC=15V, GL2=0V UT, VT, WT, UB, VB, WB=0V ICB=0A |
| | | | Is2 | BU, BV, BW | — | 15 | 30 | μA | Between BU-U, BV-V, BW-W =15V |
| 2 | Output source current | | Io+ | PGU, PGV, PGW NGU, NGV, NGW | 0.20 | 0.25 | — | A | VCC=15V, Pulse width ≤ 10μs Between BU-PGU, BV-PGV, BW-PGW=15V Between VCC-NGU, NGV, NGW=15V |
| 3 | Output sink current | | Io- | PGU, PGV, PGW NGU, NGV, NGW | 0.30 | 0.40 | — | A | VCC=15V, Pulse width ≤ 10μs Between PGU-U, PGV-V, PGW-W=15V Between NGU, NGV, NGW-GL2=15V |
| 4 | High level output voltage | | VOH | PGU, PGV, PGW NGU, NGV, NGW | — | — | 100 | mV | VCC=15V, Io+=0A Between BU-PGU, BV-PGV, BW-PGW Between VCC-NGU, NGV, NGW |
| 5 | Low level output voltage | | VOL | PGU, PGV, PGW NGU, NGV, NGW | — | — | 100 | mV | VCC=15V, Io-=0A Between PGU-U, PGV-V, PGW-W Between NGU, NGV, NGW-GL2 |
| 6 | Output delay time | Turn ON | TdONT | PGU, PGV, PGW | — | 0.4 | 1.0 | μs | VCC=15V, When connecting following capacitance: Between PGU-U, PGV-V, PGW-W=1000pF Between NGU, NGV, NGW- GL2=1000pF |
| 7 | | | TdONB | NGU, NGV, NGW | — | 0.4 | 1.0 | μs | |
| 8 | | Turn OFF | TdOFFT | PGU, PGV, PGW | — | 0.4 | 1.0 | μs | |
| 9 | | | TdOFFB | NGU, NGV, NGW | — | 0.4 | 1.0 | μs | |
| 10 | Leakage current at high voltage pin | | IL | BU, BV, BW U, V, W | — | — | 10 | μA | BU, BV, BW=U, V, W=450V |
| 11 | Over-current protection reference voltage | | Vref | RS | 0.45 | 0.50 | 0.55 | V | VCC=15V |

TABLE 2.2.1 Electrical Characteristics (1/2) Suffix (T: Top arm, B: Bottom arm) Condition: Ta=25°C

| No. | Item | Symbol | Pin | Min. | Typ. | Max. | Unit | Condition | | |
|-----|------------------------------------|-------------------|-------------|----------------------|------|------|------|--|------------------------|------------------------------|
| 12 | Over-current protection delay time | Tref | RS | — | 2.0 | 4.0 | μs | VCC=15V, When connecting following capacitance: Between PGU-U,PGV-V, PGW-W=1000pF Between NGU,NGV,NGW-GL2=1000pF | | |
| 13 | UT,VT, WT,UB, VB,WB inputs | Voltage | VIH | UT,VT,WT | 2.5 | — | — | V | VCC=15V | |
| 14 | | | VIL | UB,VB,WB | — | — | 1.0 | V | | |
| 15 | VB,WB inputs | Current | IIL | UT,VT,WT UB,VB,WB | -10 | — | — | μA | Input=0V, VCC=15V | Pull-down resistor Note 1 |
| 16 | | | IIH | | — | — | 100 | μA | Input=4.5V, VCC=15V | |
| 17 | RS input current | IILRS | RS | -100 | — | — | μA | VCC=15V, RS=0V Pull-up resistor Note 2 | | |
| 18 | VCB supply output | Voltage | VCB | CB | 4.5 | 5.0 | 5.5 | V | VCC=15V, ICB=0A | |
| 19 | | Current | ICB | CB | — | — | 45 | mA | VCC=15V | |
| 20 | LVSD | Operating voltage | LVSDON | VCC | 9.5 | 11.0 | 12.5 | V | Note 3 | |
| 21 | | Recovery voltage | LVSDOFF | | 10.0 | 11.5 | 13.0 | V | | |
| 22 | Top arm | Operating voltage | LVSDONT | BU,BV,BW | 9.0 | 10.0 | 11.0 | V | | |
| 23 | LVSD | Recovery voltage | LVSDOFFT | | 9.5 | 10.5 | 11.5 | V | | |
| 24 | F,FU,FV output resistance | RON | F,FU,FV | — | 0.4 | 0.8 | kΩ | I=-1mA Note 4 | | |
| 25 | Fault reset delay time | tflrs | F | — | 15 | 30 | μs | VCC=15V | | |
| 26 | Bootstrap diode forward voltage | VFDB | BU,BV,BW,BD | — | 1.0 | 1.5 | V | I=1mA, Between BD-BU,BV,BW Included series resistance | | |
| 27 | Back EMF detection level | VIHE | U,V | 4 | — | — | V | VCC=15V, UT,VT,WT,UB,VB,WB=0V | | |
| 28 | | VILE | | — | — | 1 | V | | | |

Note 1: Internal pull-down resistor is typically 200kΩ. The equivalent circuit is shown in FIGURE 2.2.1.

Note 2: Internal pull-up resistor is typically 260kΩ. The equivalent circuit is shown in FIGURE 2.2.2.

Note 3: The LVSD function detects and shuts down at low Vcc.

Note 4: The equivalent circuit is shown in FIGURE 2.2.3.

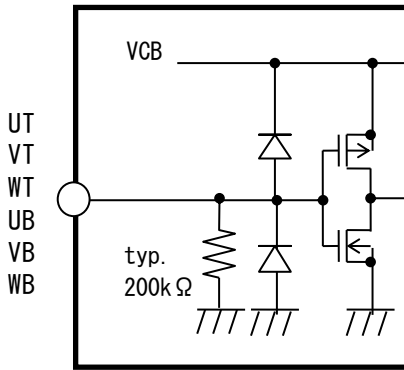


FIGURE 2.2.1 Equivalent Circuit around UT,VT,WT,UB,VB,WB Pins

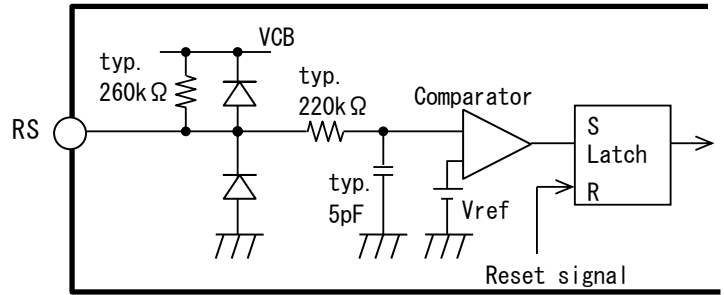


FIGURE 2.2.2 Equivalent Circuit around RS Pin

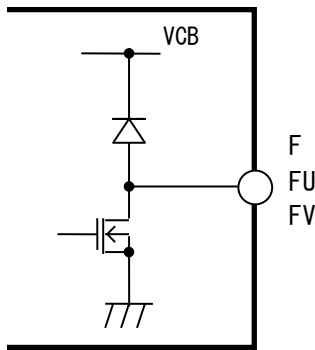


FIGURE 2.2.3 Equivalent Circuit around F, FU, FV Pins

2.3 Operating Condition

TABLE 2.3.1 Operating Condition

Condition: Ta=25°C

| No. | Item | Symbol | Pin | Min. | Typ. | Max. | Unit | Remark |
|-----|--|----------------------------|-------------------------|------|------|------|------|--|
| 1 | U, V, W voltage | VUop VVop VWop | U V W | -3 | - | 450 | V | VCC=15V Each voltage between BU-U, BV-V, BW-W: 15V |
| 2 | Supply voltage | VCCop | VCC, BD | 13.5 | 15.0 | 16.5 | V | |
| 3 | Voltage between BU-U, BV-V, BW-W | VBSUop VBSVop VBSWop | BU, U BV, V BW, W | 11.0 | 15.0 | 16.5 | V | Note 1 |

Note 1: During power supply startup, when the voltage is equal to or lower than the top arm LVSD recovery voltage, the IC may not operate.

2.4 Functions and Operations

2.4.1 Truth Table

TABLE 2.4.1.1 Truth Table

| Input UT, VT, WT UB, VB, WB | Output PGU, PGV, PGW NGU, NGV, NGW |
|-----------------------------------|--|
| L | L |
| H Note 1 | H |

Note 1: When the top input and bottom input in the same phase are "H" simultaneously, the top and bottom arm outputs in this phase become both "L".

2.4.2 Definition of Output Delay Time

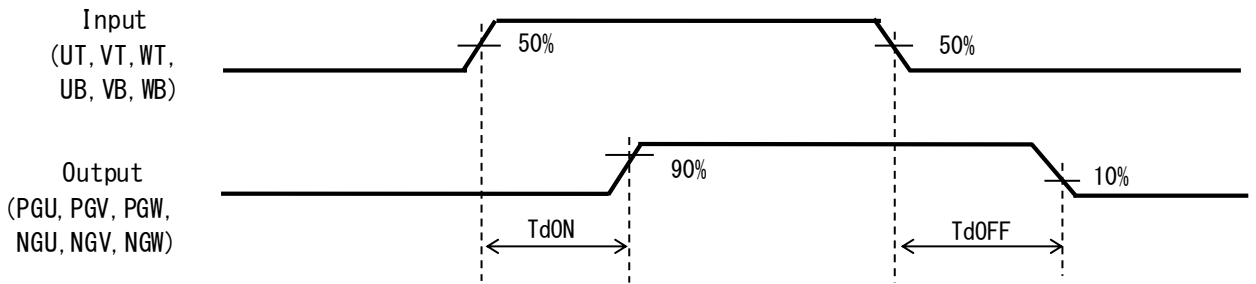


FIGURE 2.4.2.1 Definition of Output Delay Time (Capacitive Load)

2.4.3 Over-current Protection

This IC monitors the current through the shunt resistance R_s . When the voltage at the RS pin exceeds the V_{ref} (Typ. 0.5V) of the internal detection circuit, the outputs of the top and bottom arms become all "L" and the F pin outputs "L". This "All-Off" state is reset when the 6 input signals (UT, VT, WT, UB, VB, WB) are all held at "L" level for the Fault reset delay time (t_{flrs}) or longer.

Just after the V_{cc} power supply is turned on, the over current protection may operate. In this case, reset the "All-Off" state in the same way as above.

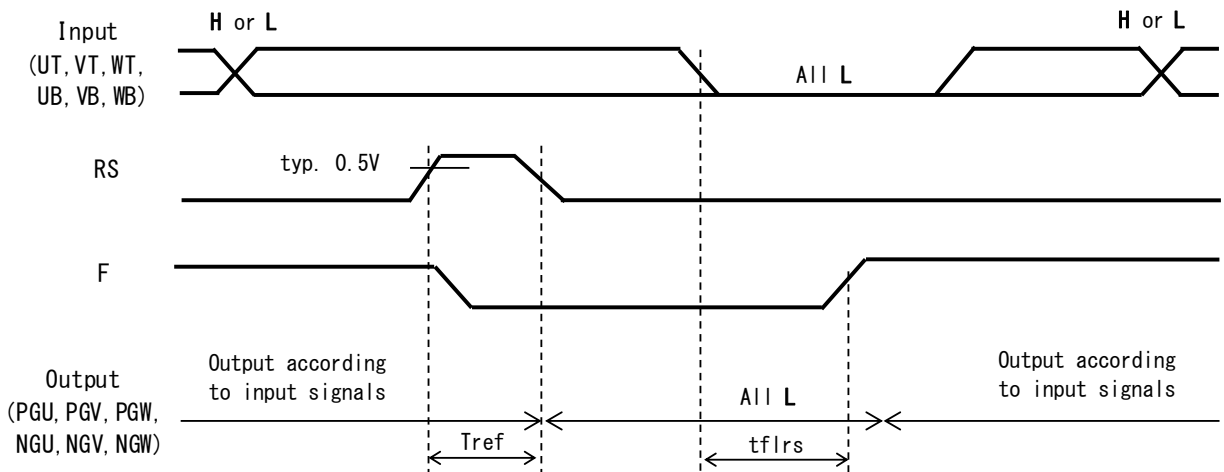


FIGURE 2.4.3.1 Timing Chart for Over-current Protection

2.4.4 Vcc Low-voltage Detection

When the Vcc voltage drops below the operating voltage of the Vcc low-voltage detection (LVSDON), the F pin outputs “L”, and the outputs of the top and bottom arms become all “L”. This “All-Off” state is reset when the 6 input signals (UT, VT, WT, UB, VB, WB) are all held at “L” level for the Fault reset delay time (tflrs) or longer.

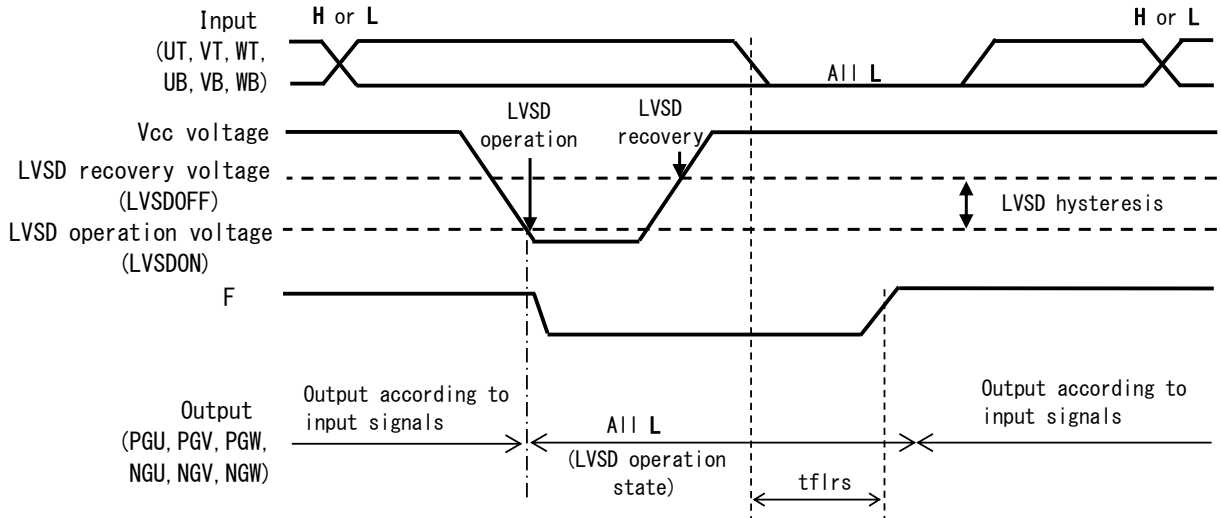


FIGURE 2.4.4.1 Timing Chart for Vcc Low-voltage Detection

2.4.5 Top Arm Low-voltage Detection

When the voltage between BU and U (BV and V, or BW and W) drops below the operating voltage of the top arm low-voltage detection (LVSDONT), the top arm output of the corresponding phase becomes “L”. This “L” output state is reset when the “H” signal is inputted to the top arm after the voltage between BU and U (BV and V, or BW and W) goes up above the recovery voltage of the top arm low-voltage detection (LVSDOFFT). The Fault signal is not outputted in this function operation.

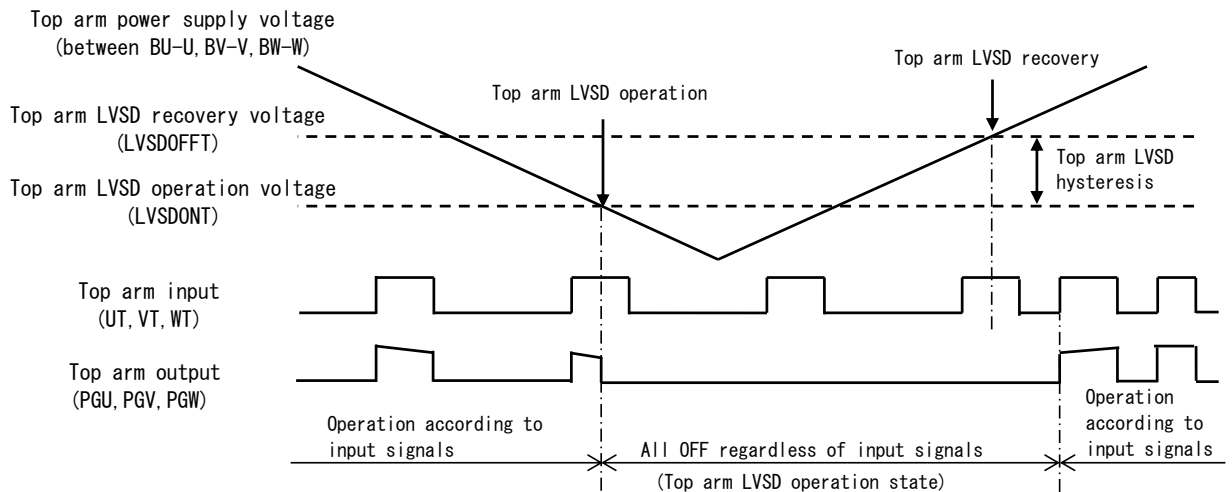


FIGURE 2.4.5.1 Timing Chart for Top Arm Low-voltage Detection

3. Standard Applications

3.1 External Components

TABLE 3.1.1 External Components

| Component | Standard value | Usage | Remark |
|--------------|-----------------|---|--------|
| Co | 1.0μF ±20%, 25V | Smooths the internal power supply (VCB) | |
| Cb | 1.0μF ±20%, 50V | For bootstrap | Note 1 |
| Rs | Note 2 | Sets over-current protection | |
| RF, RFU, RFV | 10kΩ ±5% | For pull up | |

Note 1: The capacitance value of the bootstrap capacitor depends on the operating conditions. Set the capacitance value taking into account the DC bias characteristics.

Note 2: The over-current detection setting I can be calculated as follows.

$$I = V_{ref} / R_s \text{ (A)}$$

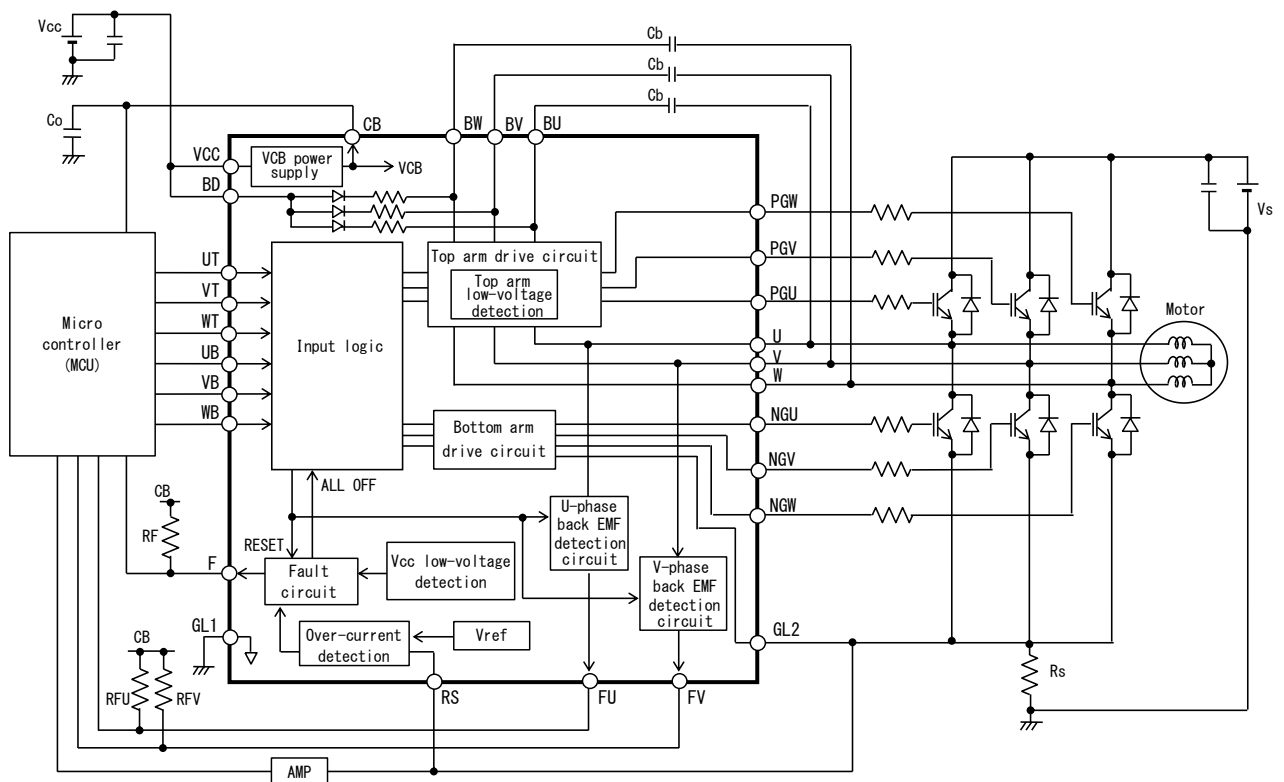


FIGURE 3.1.1 Block Diagram (ECN30552S is shown inside the bold line.)

3.2 Input Pins (UT, VT, WT, UB, VB, WB)

In some applications, input pins may be sensitive to noise due to high impedance. If noise is detected at an input pin, the following resistor and/or capacitor should be added.

- Resistor : 5.6kΩ ±5% pull-down resistor between the GL1 pin and input pins
- Capacitor : 470pF ±20% ceramic capacitor close to the input pins

4. Pin Locations

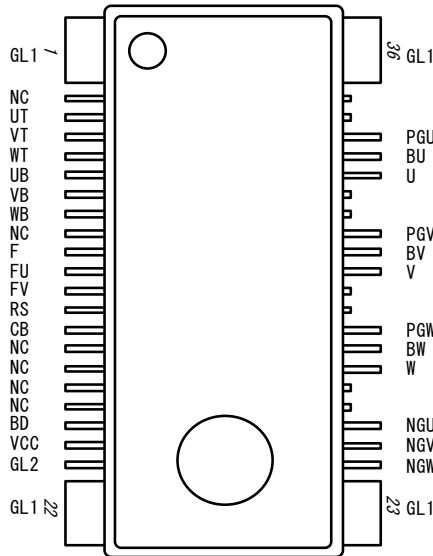


FIGURE 4.1 Pin Locations (Top view)

5. Explanations of Pins

TABLE 5.1 Explanations of Pins

| Pin No. | Symbol | Explanation | Remark |
|-----------------|--------|---|--------|
| 1,22,23,36 | GL1 | Control system GND | |
| 2,9,15,16,17,18 | NC | No connection | Note 2 |
| 3 | UT | Input control signal for U-phase top arm | |
| 4 | VT | Input control signal for V-phase top arm | |
| 5 | WT | Input control signal for W-phase top arm | |
| 6 | UB | Input control signal for U-phase bottom arm | |
| 7 | VB | Input control signal for V-phase bottom arm | |
| 8 | WB | Input control signal for W-phase bottom arm | |
| 10 | F | Fault signal output | |
| 11 | FU | U-phase back EMF feedback signal output | |
| 12 | FV | V-phase back EMF feedback signal output | |
| 13 | RS | Rs voltage input for over-current detection | |
| 14 | CB | VCB power supply output | |
| 19 | BD | For bootstrap diode | |
| 20 | VCC | 15V control power supply | |
| 21 | GL2 | Reference pin of bottom arm outputs (connected to a current detection resistor) | |
| 24 | NGW | W-phase bottom arm gate drive signal output | |
| 25 | NGV | V-phase bottom arm gate drive signal output | |
| 26 | NGU | U-phase bottom arm gate drive signal output | |
| 27 | W | Reference pin of W-phase top arm output | Note 1 |
| 28 | BW | W-phase top arm driving circuit power supply | Note 1 |
| 29 | PGW | W-phase top arm gate drive signal output | Note 1 |
| 30 | V | Reference pin of V-phase top arm output | Note 1 |
| 31 | BV | V-phase top arm driving circuit power supply | Note 1 |
| 32 | PGV | V-phase top arm gate drive signal output | Note 1 |
| 33 | U | Reference pin of U-phase top arm output | Note 1 |
| 34 | BU | U-phase top arm driving circuit power supply | Note 1 |
| 35 | PGU | U-phase top arm gate drive signal output | Note 1 |

Note 1: High voltage pin.

Note 2: Not connected to the chip in the IC.

6. Inspection

Hundred percent inspections shall be conducted on electric characteristics at room temperature.

7. Precautions for Use

7.1 Countermeasures against Electrostatic Discharge (ESD)

- (a) Customers need to take precautions to protect ICs from electrostatic discharge (ESD). The material of the container or any other device used to carry ICs should be free from ESD, which can be caused by vibration during transportation. Use of electrically conductive containers is recommended as an effective countermeasure.
- (b) Everything that touches ICs, such as the work platform, machine, measuring equipment, and test equipment, should be grounded.
- (c) Workers should be high-impedance grounded (100kΩ to 1MΩ) while working with ICs, to avoid damaging the ICs by ESD.
- (d) Friction with other materials, such as high polymers, should be avoided.
- (e) When carrying a PCB with a mounted IC, ensure that the electric potential is maintained at a constant level using the short-circuit terminals and that there is no vibration or friction.
- (f) The humidity at an assembly line where ICs are mounted on circuit boards should be kept around 45 to 75 percent using humidifiers or such. If the humidity cannot be controlled effectively, using ionized air blowers (ionizers) is effective.

7.2 Maximum Ratings

Regardless of changes in external conditions during use of this IC (the product of Hitachi Power Semiconductor Device, hereinafter called "HPSD's IC"), the "maximum ratings" described in this document should never be exceeded when designing electronic circuits that employ HPSD's IC. If maximum ratings are exceeded, HPSD's IC may be damaged or destroyed. In no event shall Hitachi Power Semiconductor Device (hereinafter called "HPSD") be liable for any failure in HPSD's IC or any secondary damage resulting from use at a value exceeding the maximum ratings.

7.3 Derating Design

Continuous high-load operation (high temperatures, high voltages, large currents) should be avoided and derating design should be applied, even within the ranges of the maximum ratings, to ensure reliability.

7.4 Safe Design

The HPSD's IC may fail due to accidents or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy and measures to prevent misuse, in order to avoid extensive damage in the event of a failure.

7.5 Application

If HPSD's IC is applied to the following uses where high reliability is required, obtain the document of permission from HPSD in advance.

- Automobile, Train, Vessel, etc.

Do not apply HPSD's IC to the following uses where extremely high reliability is required.

- Nuclear power control system, Aerospace instrument, Life-support-related medical equipment, etc.

7.6 Soldering

(1) Soldering Condition

The recommended reflow soldering condition is shown in FIGURE 7.6.1.

High stress by mounting, such as long time thermal stress by preheating, mechanical stress, etc., can lead to degradation or destruction. Make sure that your mounting method does not cause problem as a system.

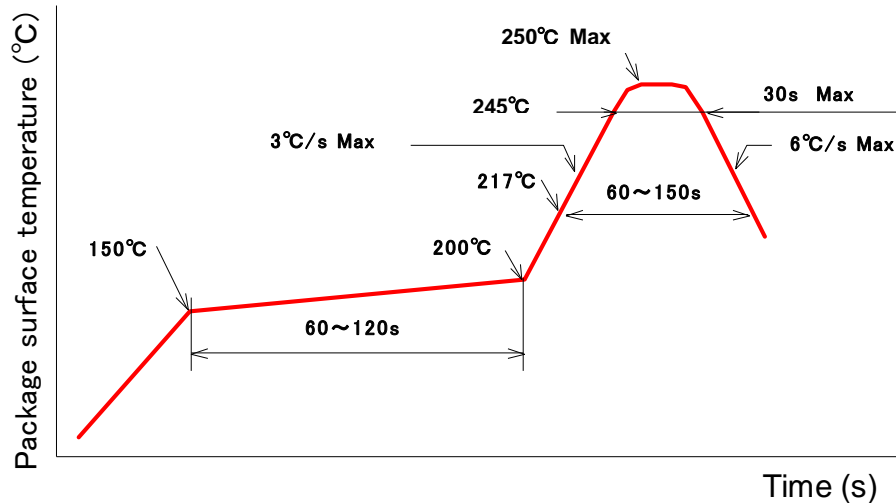


FIGURE 7.6.1 Recommended Conditions for Infrared Reflow or Air Reflow

(2) Reliability of Solder Connection

The reliability of solder connection depends on soldering condition, materials of circuit boards, footprint, etc. Test it sufficiently by heat cycle test, heat shock test, and so on after mounting ICs on circuit boards.

7.7 Storage Conditions

(1) Before opening the moisture prevention bag (aluminum laminate bag)

Temperature: less than 40°C
Humidity: less than 90%RH
Period: less than 12 months

(2) After opening the moisture prevention bag (aluminum laminate bag)

Temperature: 5°C to 30°C
Humidity: less than 60%RH
Period: less than 168 hours

※ When the period of (1) and (2) is likely to expire, store the IC in a drying furnace (10%RH or lower) at ordinary temperature.

(3) Baking process

When the period of (1) and (2) has expired, the IC should be baked in accordance with the following conditions. (However, when the IC is stored in a drying furnace (10%RH or lower) at ordinary temperature, there is no need to bake.) Do not bake the tape and the reel of the taping package because they are not heat resistant. Transfer the IC to a heat resistant container prior to baking.

Temperature: 125°C to 135°C
Period: more than 48 hours

7.8 Others

See “Instructions for Use of Hitachi High-Voltage Monolithic ICs” and “Application Note” for other precautions and instructions on how to deal with these kinds of products.

8. Usage

- (1) HPSD warrants that the HPSD products have the specified performance according to the respective specifications at the time of its sale. Testing and other quality control techniques of the HPSD products by HPSD are utilized to the extent HPSD needs to meet the specifications described in this document. Not every device of the HPSD products is specifically tested on all parameters, except those mandated by relevant laws and/or regulations.
- (2) Following any claim regarding the failure of a product to meet the performance described in this document made within one month of product delivery, all the products in relevant lot(s) shall be re-tested and re-delivered. The HPSD products delivered more than one month before such a claim shall not be counted for such response.
- (3) HPSD assumes no obligation nor makes any promise of compensation for any fault which should be found in a customer's goods incorporating the products in the market. If a product failure occurs for reasons obviously attributable to HPSD and a claim is made within six months of product delivery, HPSD shall offer free replacement or payment of compensation. The maximum compensation shall be the amount paid for the products, and HPSD shall not assume responsibility for any other compensation.
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◆ Appendix - Supplementary Data

1. Dimensions

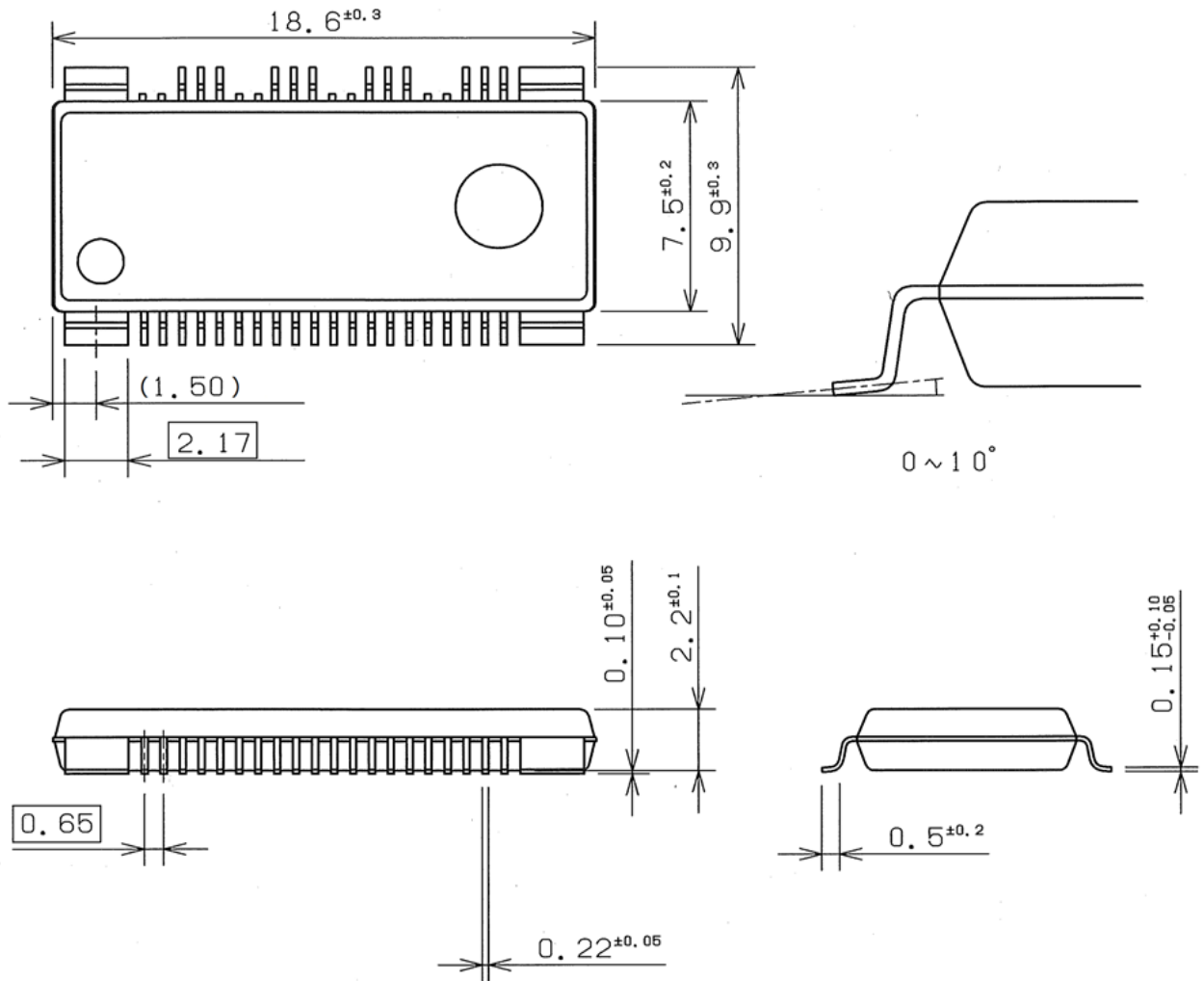


FIGURE A: Dimensions

Unit: mm

2. External Packaging

2.1 External Packaging

FIGURE B shows the external packaging. Order quantities are basically multiples of 2000.

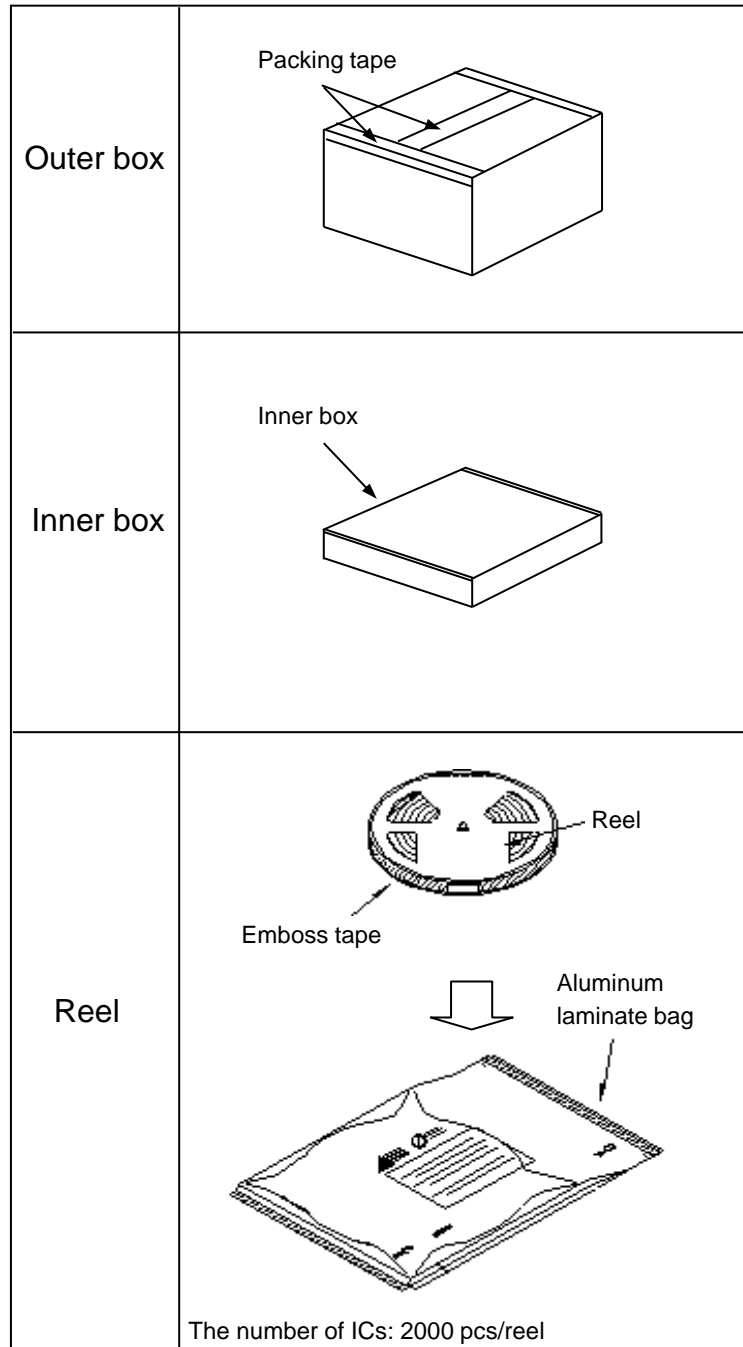


FIGURE B: External Packaging

Precautions for Safe Use and Notices

If semiconductor devices are handled in an inappropriate manner, failures may result. For this reason, be sure to read the latest version of "Instructions for Use of Hitachi High-Voltage Monolithic ICs" before use.



This mark indicates an item requiring caution.



CAUTION

This mark indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury and damage to property.



CAUTION

- (1) Regardless of changes in external conditions during use of semiconductor devices, the "maximum ratings" and "safe operating area(SOA)" should never be exceeded when designing electronic circuits that employ semiconductor devices.
- (2) Semiconductor devices may fail due to accidents or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy and measures to prevent misuse, in order to avoid extensive damage in the event of a failure.
- (3) If semiconductor devices are applied to uses where high reliability is required, obtain the document of permission from HPSD in advance (Automobile, Train, Vessel, etc.). Do not apply semiconductor devices to uses where extremely high reliability is required (Nuclear power control system, Aerospace instrument, Life-support-related medical equipment, etc.).
(If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

NOTICES

1. This Data Sheet contains the specifications, characteristics, etc. concerning power semiconductor products (hereinafter called "products").
2. All information included in this document such as product data, diagrams, charts, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, specifications of products, etc. are subject to change without prior notice. Before purchasing or using any of the HPSD products listed in this document, please confirm the latest product information with a HPSD sales office.
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