

8-channel High Voltage analog switch IC

ECN3293TF Product Specification

Rev.3

ECN3293 is an eight-channel High Voltage analog switching IC with bleed resistors on which latch-up free is realized by dielectric isolation technology.

High voltage and low ON-resistance MOS switches are used as output devices controlled by a 3.3V or 5V signal. The ECN3293 is most suited to Ultrasound Imaging applications.

Functions

- * High voltage and low on-resistance MOS switches integrated.
- * 8bit shift register integrated.
- * Integrated bleed resistors on the outputs.

Features

- * Switch on-resistance: 19 Ω typ. ($V_{PP}=100V, V_{NN}=-100V, I_{SIG}=5mA, 25^{\circ}C$)
- * Switch breakdown voltage: 220V
- * Latch-up free CMOS and High-Voltage drive circuit.
- * Power on/off sequence of power supply is free.

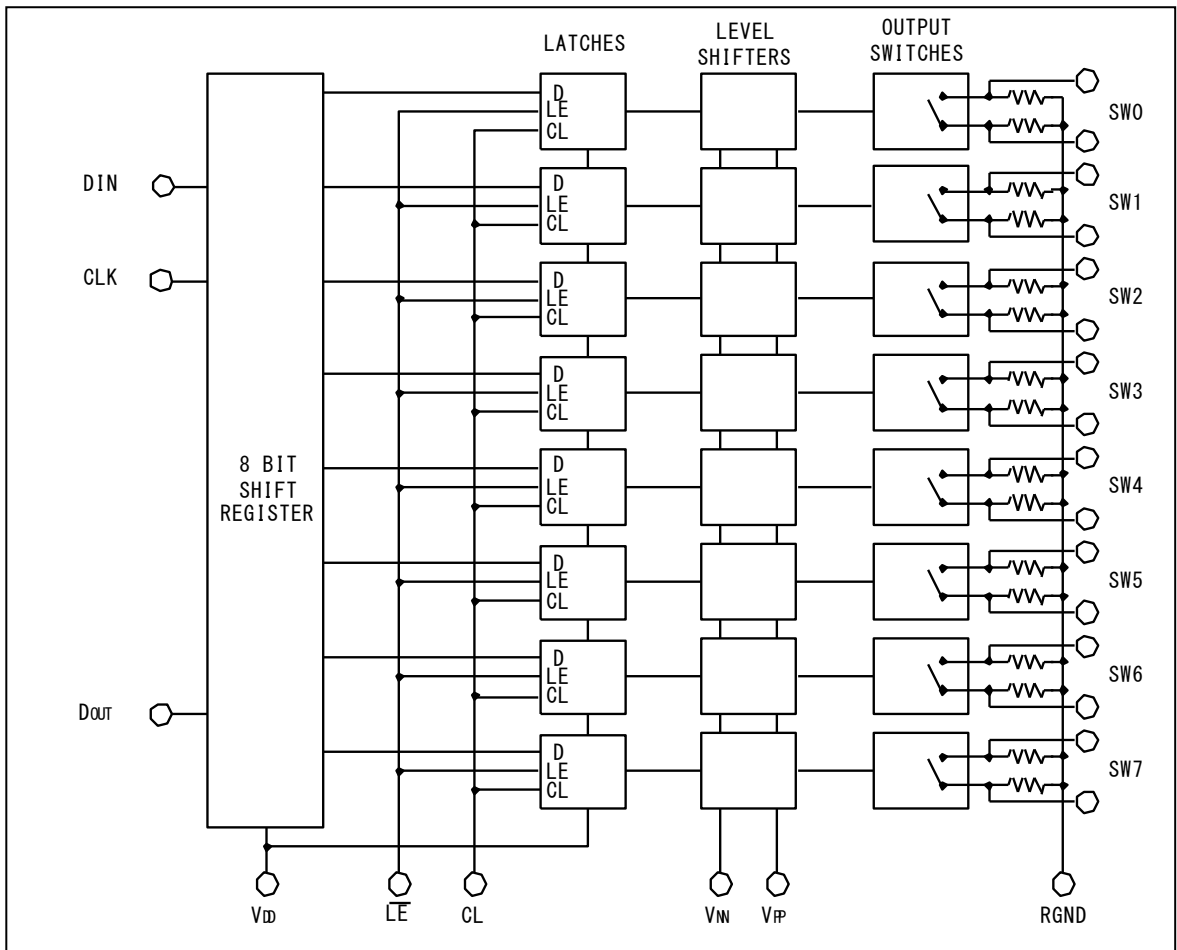


Fig.1 Block diagram

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1. General

This Specification shall be applied to the following semiconductor integrated circuit.

- 1) Parts name : ECN3293TF
- 2) Application : Ultrasound imaging scanner and others
- 3) Structure : Monolithic IC
- 4) Package : LQFP48

2. Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Terminal	Values	Unit	Note
1	Logic power supply voltage	VDD	VDD	-0.5 ~ +7V	V	Ta=25°C
2	VPP-VNN supply voltage	-	VPP, VNN	220V	V	Ta=25°C
3	VPP Positive high voltage supply	VPP	VPP	-0.5 to VNN+200V	V	Ta=25°C
4	VNN negative high voltage supply	VNN	VNN	+0.5 to -200V	V	Ta=25°C
5	Logic input voltages	VDD	DIN, CLK, CL, LE	-0.5 to VDD+0.3	V	Ta=25°C
6	Analog signal range	-	SW0 to SW7	VNN to VPP	V	Ta=25°C
7	Operating junction temperature	Tjop	-	-20 to +125	°C	
8	Storage temperature	Tstg	-	-65 to +150	°C	
9	Power dissipation	Pw	-	1.0	W	LQFP48 Ta=70°C

3. Electrical Characteristics

3.1 DC Characteristics

Table 2 DC Characteristics

Ta=25°C VDD=5V

No.	Items	Symbol	Spec			Unit	Test conditions	
			Min	Typ	Max			
1	Small signal switch on resistance	RONS	-	24	38	Ω	I SIG=5mA	VPP=40V, VNN=-160V
			-	17	27		I SIG=200mA	VNN=-100V
			-	19	27		I SIG=5mA	VPP=100V, VNN=-100V
			-	15	24		I SIG=200mA	VNN=-100V
			-	19	25		I SIG=5mA	VPP=160V, VNN=-40V
			-	15	25		I SIG=200mA	VNN=-40V
2	Small signal switch on resistance matching	ΔRONS	-	5	20	%	VPP=100V, VNN=-100V ISW=5mA	
3	Large signal switch on resistance	RONL	-	16	—	Ω	VPP=100V VNN=-100V	I SIG=1A
4	Value of output bleed resistance	RINT	20	35	50	kΩ	Output switch to RGND IRINT=0.5mA	
5	Switch off leakage per switch	ISOL	-	1.0	10	μA	VSIG=VPP-10V, or VNN+10V	
6	DC offset switch (off)	DCOFF	-	10	100	mV	No load	
7	DC offset switch (on)	DCON	-	10	100	mV	No load	
8	Positive HV supply current	IPPQ1	-	10	50	μA	All SWs off	
9	Negative HV supply current	INNQ1	-	-10	-50	μA	All SWs off	
10	Positive HV supply current	IPPQ2	-	10	50	μA	All SWs on, ISW=5mA	
11	Negative HV supply current	INNQ2	-	-10	-50	μA	All SWs on, ISW=5mA	
12	IPP Supply current	IPP	-	-	7.0	mA	VPP=40V VNN=-160V	50kHz output switching frequency without load
			-	-	5.0		VPP=100V VNN=-100V	
			-	-	5.0		VPP=160V VNN=-40V	
13	INN Supply current	INN	-	-	7.0	mA	VPP=40V VNN=-160V	50kHz output switching frequency without load
			-	-	5.0		VPP=100V VNN=-100V	
			-	-	5.0		VPP=160V VNN=-40V	
14	Logic supply average current	IDD	-	-	4.0	mA	fCLK=5MHz, VDD=5.0V	
15	Logic supply quiescent current	IDDQ	-	-	10	μA		
16	Data out source current	ISOR	0.45	0.70	-	mA	VOUT= VDD-0.7V	
17	Data out sink current	ISINK	0.45	0.70	-	mA	VOUT=0.7V	

3.2 AC Characteristics

Table 3 AC Characteristics

Ta=25°C VDD=5V

No.	Items	Symbol	Spec			Unit	Test conditions
			Min	Typ	Max		
1	SW Turn on time	tON	-	-	5.0	μs	VSIG=VPP-10V, RL=10kΩ
2	SW Turn off time	tOFF	-	-	5.0	μs	VSIG=VPP-10V, RL=10kΩ
3	Clock frequency	fCLK	-	-	20	MHz	50% duty cycle, fData=fCLK/2 VDD=3.0V or 5.0V
4	Clock delay time to data out	tDO	30	-	110	ns	DOUT terminal, VDD=3.0V
			20	-	70	ns	DOUT terminal, VDD=5.0V
5	Output voltage spike	+VSPK	-	-	150	mV	VPP=40V, VNN=-160V, RL=50Ω
		-VSPK	-	-	-200		
		+VSPK	-	-	150		VPP=100V, VNN=-100V, RL=50Ω
		-VSPK	-	-	-200		
		+VSPK	-	-	150		VPP=160V, VNN=-40V, RL=50Ω
		-VSPK	-	-	-200		

Table 4 AC Characteristics (for reference purpose only)

Ta=25°C VDD=5V

No.	Items	Symbol	Spec			Unit	Condition
			Min	Typ	Max		
1	Off capacitance SW to GND	CSG (off)	-	9	-	pF	0V, 1MHz
2	On Capacitance SW to GND	CSG (on)	-	14	-	pF	0V, 1MHz
3	SW off isolation	KO	-30	-33	-	dB	f=5MHz, 1kΩ//15pF load
			-54	-60	-	dB	f=5MHz, 50Ω load
4	SW Crosstalk	KCR	-54	-60	-	dB	f=5MHz, 50Ω load

Note: These items are not tested when shipped.

4. Recommended Operating Conditions

Please operate in use within the limit of recommended operating conditions detailed in Table 5.

Table 5 Recommended Operating Conditions

No	Items	Symbol	Recommended Value
1	Logic power supply voltage	VDD	3.0V to 5.5V
2	Positive high voltage supply	VPP	40V to VNN+200V
3	Negative high voltage supply	VNN	-40V to -160V
4	High-level input voltage	VIH	0.9VDD to VDD
5	Low-level input voltage	VIL	0V to 0.1VDD
6	Analog signal voltage peak to peak	VSIG	VNN+10V to VPP-10V
7	Operating free air-temperature	Ta	0°C to 70°C
8	Switching frequency	Fsw	50kHz max, Duty Cycle=50%
9	Set up time for LE	TSD	Min.75ns
10	Pulse width of LE	TWLE	Min.75ns
11	Time width of CL	TWCL	Min.60ns
12	Set up time DATA to Clock	TSU	Min.10ns
13	Hold time DATA from Clock	Th	Min.20ns
14	Maximum VSIG Slew Rate	dV/dt	Max.30V/ns

Attention ;

- 1) Power on/off sequence of power supply is arbitrary except GND terminal of IC must be powered-up first and powered-down last.
- 2) It is indispensable to make there are not to exceed a maximum rated voltage by the occurrence of the excessive voltage in case of investing and cutting of the power supply.

5. Test Circuit

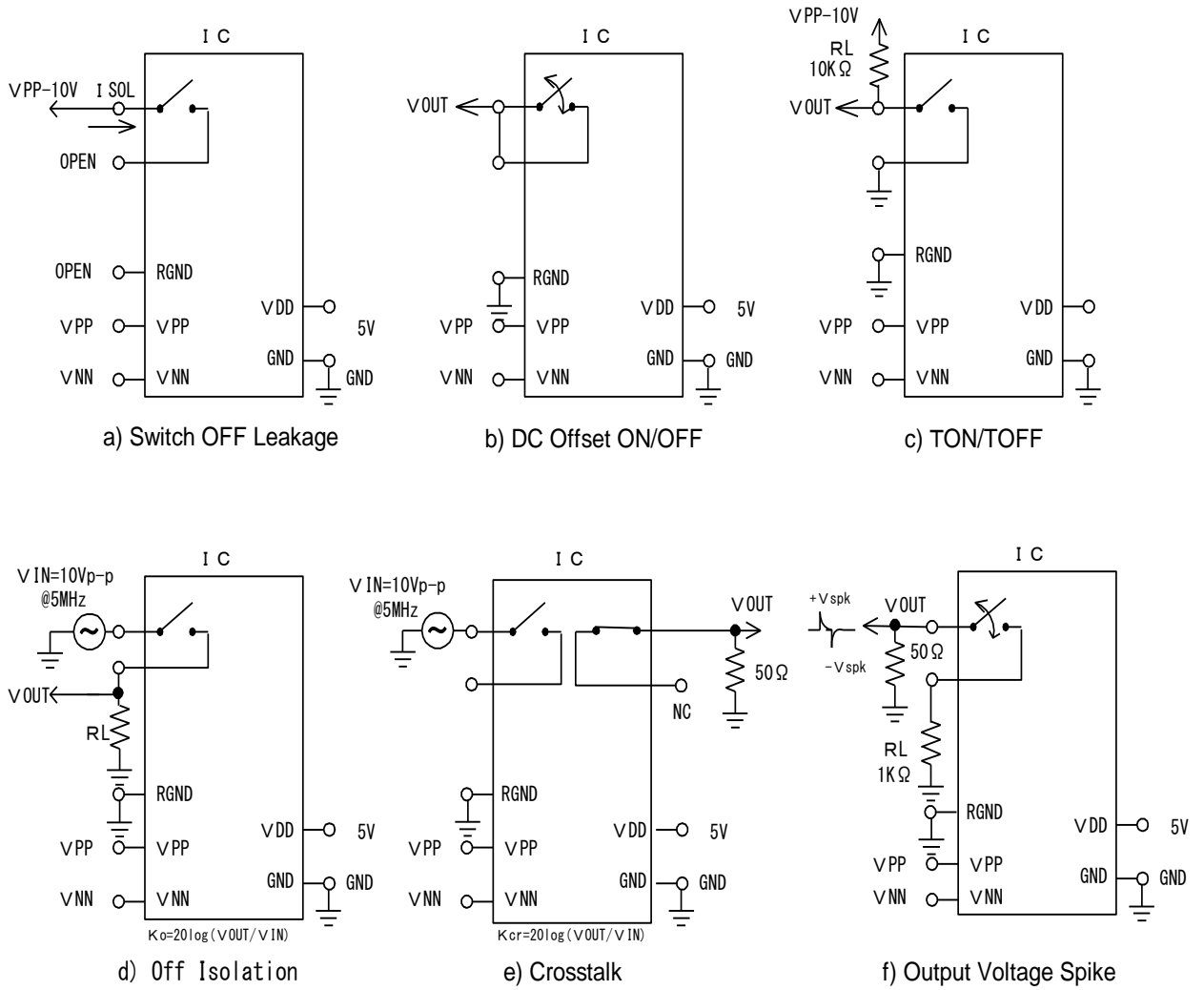


Fig. 2 Test Circuit

6. Timing Waveforms

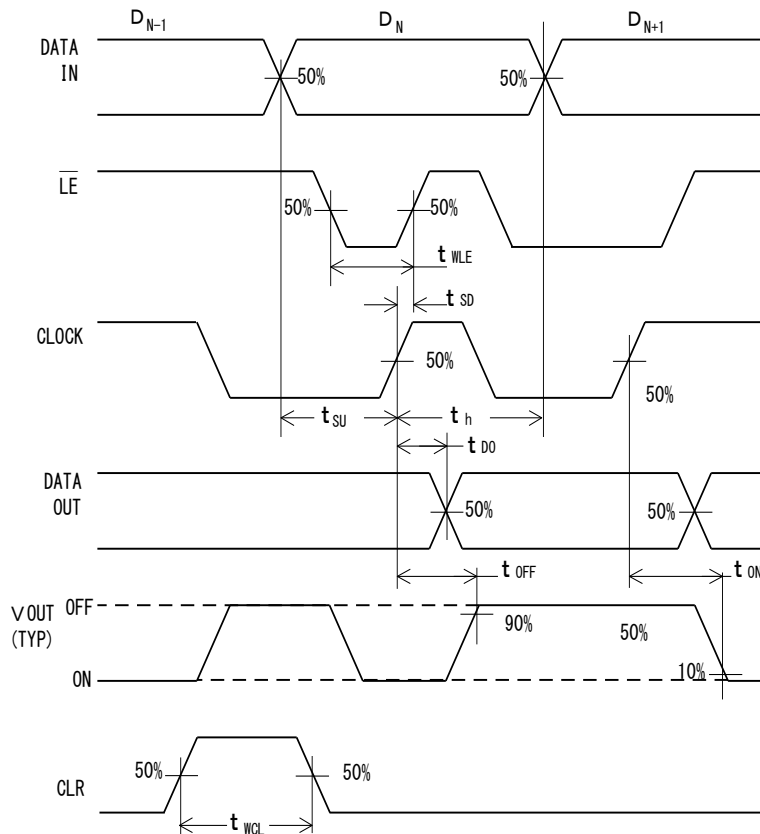


Fig. 3 Timing Waveforms

Note

1. Serial data is clocked in on the rising edge of CLK.
2. The switches go to a state retaining their present condition on the rising edge of LE.

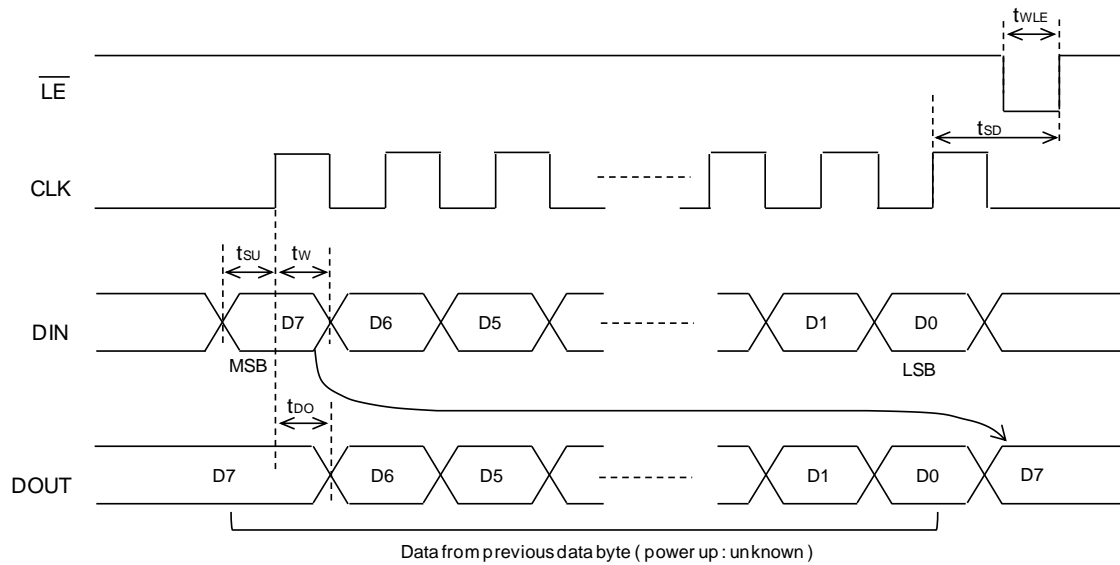


Fig. 4 LATCH ENABLE Timing Waveform

7. Truth Table

Table 6 Truth table

D0	D1	D2	D3	D4	D5	D6	D7	LE	CL	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7	
L								L	L	OFF								
H								L	L	ON								
	L							L	L		OFF							
	H							L	L		ON							
		L						L	L			OFF						
		H						L	L			ON						
			L					L	L				OFF					
			H					L	L				ON					
				L				L	L					OFF				
				H				L	L					ON				
					L			L	L						OFF			
					H			L	L						ON			
						L		L	L							OFF		
						H		L	L							ON		
							L	L	L								OFF	
							H	L	L								ON	
X	X	X	X	X	X	X	X	H	L	Hold previous state								
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

X = Don't care

Note

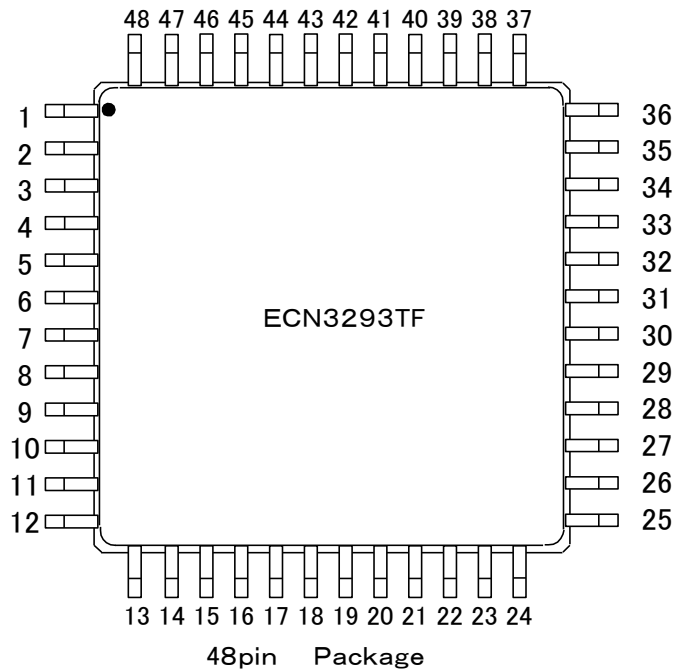
1. The 16 Switches operate independently.
2. When LE is low, the shift register data flows through the latch.
3. Shift register clocking has no effect on the switch states if LE is high.
4. When switch 15 is ON, DOUT is high.
5. The clear input overrides all other inputs.

8. Pin Configuration

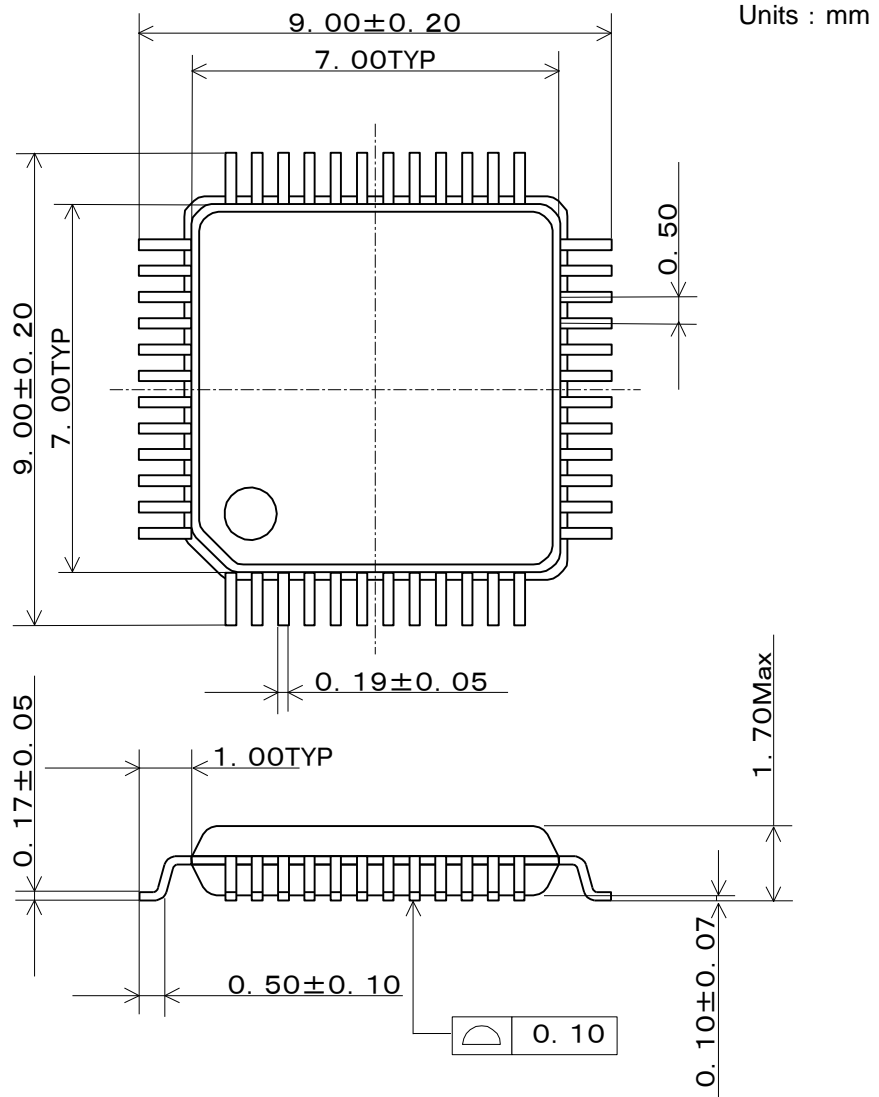
ECN3293TF LQFP48 (48Pin LQFP)

Table3. Pin Configuration

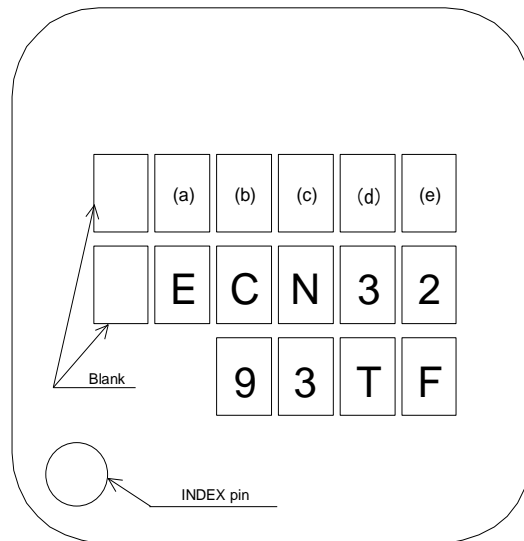
Pin	Functions	Pin	Functions
1	SW5	25	VNN
2	N/C	26	N/C
3	SW4	27	RGND
4	N/C	28	GND
5	SW4	29	VDD
6	N/C	30	N/C
7	N/C	31	N/C
8	SW3	32	N/C
9	N/C	33	DIN
10	SW3	34	CLK
11	N/C	35	\overline{LE}
12	SW2	36	CLR
13	N/C	37	DOUT
14	SW2	38	N/C
15	N/C	39	SW7
16	SW1	40	N/C
17	N/C	41	SW7
18	SW1	42	N/C
19	N/C	43	SW6
20	SW0	44	N/C
21	N/C	45	SW6
22	SW0	46	N/C
23	N/C	47	SW5
24	VPP	48	N/C



9. Package Outline



10. Marking spec



Lot numbering rule

(a) :Year code (Least significant digit of Assembled year (A.D.))

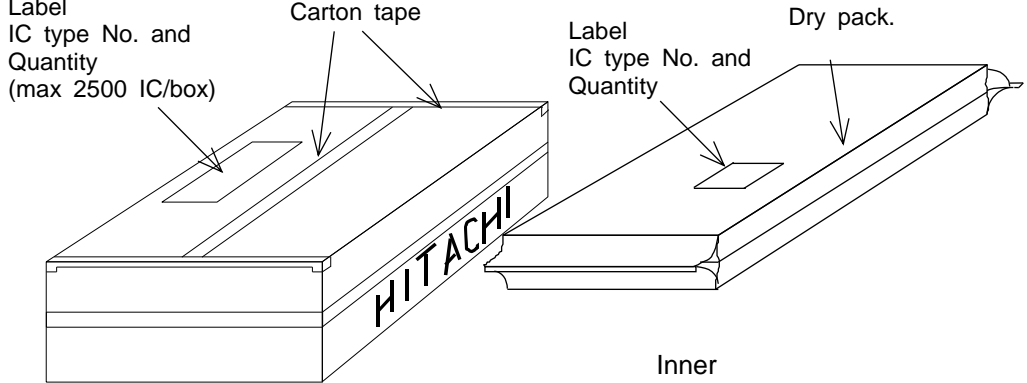
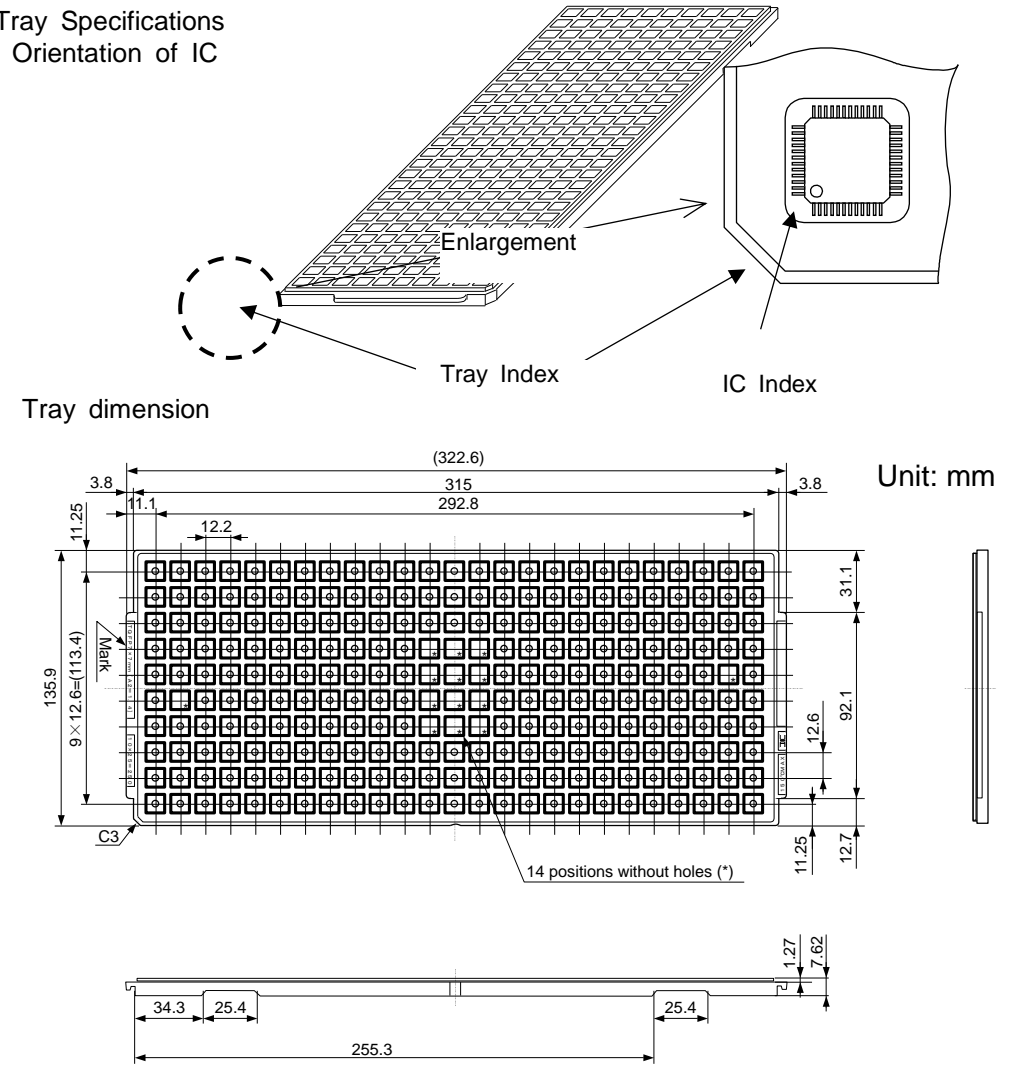
(b) :Month code (Refer to following table.)

Month	1	2	3	4	5	6	7	8	9	10	11	12
Month code	A	B	C	D	E	K	L	M	N	X	Y	Z

(c),(d),(e) :Serial number within year/month code

11. Packing Form

Packaging details are as shown below.

<p>1.Outer and inner packing</p>	 <p>Outer box (cardboard box)</p>
<p>2.Tray</p>	<p>Tray Specifications Orientation of IC</p>  <p>Tray dimension</p> <p>Unit: mm</p> <p>(322.6) 315 292.8</p> <p>3.8 11.1 12.2 11.25 135.9 9 × 12.6 = (113.4) Mark C3 3.8 31.1 12.6 92.1 11.25 12.7</p> <p>14 positions without holes (*)</p> <p>34.3 25.4 25.4 255.3 1.27 7.62</p> <p>(1) Material of tray is PPE containing carbon and static proof. (2) Packing quantity is max 250 IC/Tray. (3) Maximum heat resistant temperature is 150deg.</p>

12. Inspection

Hundred percent inspections shall be conducted on electric characteristics.

13. Precautions for use

13.1 Countermeasures against Electrostatic Discharge (ESD)

- (a) Customers need to take precautions to protect ICs from electrostatic discharge (ESD). The material of the container or any other device used to carry ICs should be free from ESD, which can be caused by vibration during transportation. Use of electrically conductive containers is recommended as an effective countermeasure.
- (b) Everything that touches ICs, such as the work platform, machine, measuring equipment, and test equipment, should be grounded.
- (c) Workers should be high-impedance grounded (100kΩ to 1MΩ) while working with ICs, to avoid damaging the ICs by ESD.
- (d) Friction with other materials, such as high polymers, should be avoided.
- (e) When carrying a PCB with a mounted IC, ensure that the electric potential is maintained at a constant level using the short-circuit terminals and that there is no vibration or friction.
- (f) The humidity at an assembly line where ICs are mounted on circuit boards should be kept around 45 to 75 percent using humidifiers or such. If the humidity cannot be controlled effectively, using ionized air blowers (ionizers) is effective.

13.2 Maximum ratings

Regardless of changes in external conditions during use IC (the product of Hitachi Power Semiconductor Device, hereinafter called "HPSD's IC"), the "maximum ratings" described in this document should never be exceeded when designing electronic circuits that employ HPSD's IC. If maximum ratings are exceeded, HPSD's IC may be damaged or destroyed. In no event shall Hitachi Power Semiconductor Device (hereinafter called "HPSD") be liable for any failure in HPSD's IC or any secondary damage resulting from use at a value exceeding the maximum ratings.

13.3 Derating Design

Continuous high-load operation (high temperatures, high voltages, large currents) should be avoided and derating design should be applied, even within the ranges of the maximum ratings, to ensure reliability.

13.4 Safe Design

The HPSD's IC may fail due to accidents or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy and measures to prevent misuse, in order to avoid extensive damage in the event of a failure.

13.5 Application

If HPSD's IC is applied to the following uses where high reliability is required, obtain the document of permission from HPSD in advance.

- Automobile, Train, Vessel, etc.

Do not apply HPSD's IC to the following uses where extremely high reliability is required.

- Nuclear power control system, Aerospace instrument, Life-support-related medical equipment, etc.

13.6 Soldering

Lead-free solder is used for coating pins and the tab of this IC.

Refer to "Precautions for Use of High Voltage Monolithic Ics" for soldering conditions.

13.7 Others

See "Instructions for Use of Hitachi High-Voltage Monolithic ICs" for other precautions and instructions on how to deal with these kinds of products.

14. Usage

- (1) HPSD warrants that the HPSD products have the specified performance according to the respective specifications at the time of its sale. Testing and other quality control techniques of the HPSD products by HPSD are utilized to the extent HPSD needs to meet the specifications described in this document. Not every device of the HPSD products is specifically tested on all parameters, except those mandated by relevant laws and/or regulations.
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Precautions for Safe Use and Notices

If semiconductor devices are handled in an inappropriate manner, failures may result. For this reason, be sure to read the latest version of "Instructions for Use of Hitachi High-Voltage Monolithic ICs" before use.



This mark indicates an item requiring caution.



CAUTION

This mark indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury and damage to property.



CAUTION

- (1) Regardless of changes in external conditions during use of semiconductor devices, the "maximum ratings" and "safe operating area(SOA)" should never be exceeded when designing electronic circuits that employ semiconductor devices.
- (2) Semiconductor devices may fail due to accidents or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy and measures to prevent misuse, in order to avoid extensive damage in the event of a failure.
- (3) If semiconductor devices are applied to uses where high reliability is required, obtain the document of permission from HPSD in advance (Automobile, Train, Vessel, etc.). Do not apply semiconductor devices to uses where extremely high reliability is required (Nuclear power control system, Aerospace instrument, Life-support-related medical equipment, etc.).
(If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

NOTICES

1. This Data Sheet contains the specifications, characteristics, etc. concerning power semiconductor products (hereinafter called "products").
2. All information included in this document such as product data, diagrams, charts, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, specifications of products, etc. are subject to change without prior notice. Before purchasing or using any of the HPSD products listed in this document, please confirm the latest product information with a HPSD sales office.
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7. In no event shall HPSD be liable for any failure in HPSD products or any secondary damage resulting from use at a value exceeding the maximum ratings.

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