3-Phase IGBT/MOS Gate Driver IC

ECN33550/ECN33500/ECN30551

Application Note

【Rev 0】

Hitachi Power Semiconductor Device, Ltd.

－ Contents －

1. Outline

1.1 3-Phase IGBT/MOS Gate Driver IC (ECN33550/33500/30551) Outline

These gate driver ICs are the monolithic ICs integrating various devices and circuits, needed for inverter control, onto a single chip by using SOI technology. They are the ICs for driving gates of a three-phase bridge inverter circuit using MOSFETs (Metal Oxide Semiconductor Field Effect Transistor), IGBTs (Insulated Gate Bipolar Transistor) or other devices. The gate driver ICs are particularly suited for variable speed control of three-phase induction motor or DC brushless motor rated operating voltage ranging from AC200V to AC240V.

The ECN33550, ECN33500, and ECN30551 are divided into two types of input (3-input/6-input). They have a back EMF detection function or a current polarity detection function to feed back the motor information to a microcomputer (hereinafter called “MCU”). Table 1.1.1 shows the differences in ECN33550, ECN33500 and ECN30551.

TABLE 1.1.1 Difference in ECN33550, ECN33500, ECN30551

Sales name (model)	Input type	Back EMF detection function	Current polarity detection function
ECN33550	3-input (*)	Yes	No
ECN33500	3-input (*)	No	Yes
ECN30551	6-input	Yes	No

* The 3-input type products generate six top and bottom arm gate drive signals with dead time from three input signals.

1.2 System Configuration

An inverter is a device that converts DC currents into AC. It can be used to drive motors for efficient variable-speed control. Fig. 1.2.1 shows the example of basic system configuration. The gate driver IC outputs the gate drive signals in accordance with the PWM signals from the MCU and drives an output power device consisting of six MOSFETs or IGBTs by the inverter.

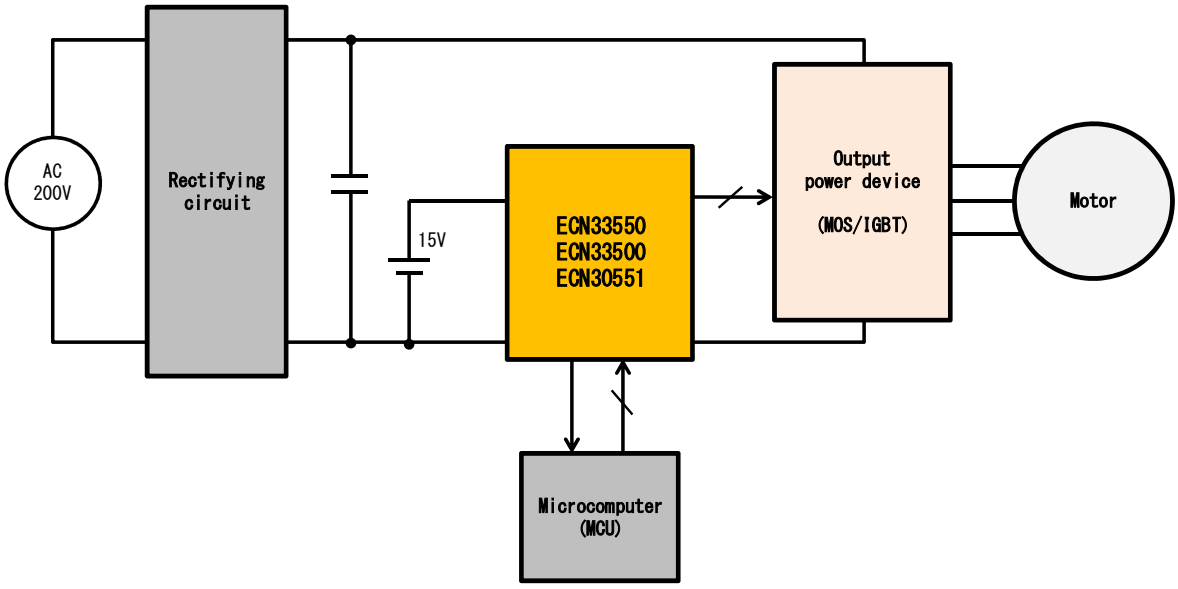


FIGURE 1.2.1 Example of Basic System Configuration

The gate driver ICs can control three-phase motors with a motor output of up to 750W class at variable speed. The standard applicable motor output of a three-phase induction motor can be generally calculated using the following formula:

$$\text{Motor output} = \sqrt{3} \times V_S \times I_M \times \cos\phi \times \eta$$

Vs : DC voltage, I_M : Motor current, cosΦ : Power factor ≈ 0.8, η : Motor efficiency ≈ 0.8

1.3 Block Diagram

Figures 1.3.1, 1.3.2 and 1.3.3 show the block diagrams. Each of the gate driver ICs is shown inside the bold line. The following devices and circuits are incorporated.

- Diodes for boot strap
- Dead time generation circuit (applied to the ECN33550, ECN33500)
- Feedback circuit for motor information (Back EMF detection circuit: ECN33550, ECN30551)
  (Current polarity detection circuit: ECN33500)

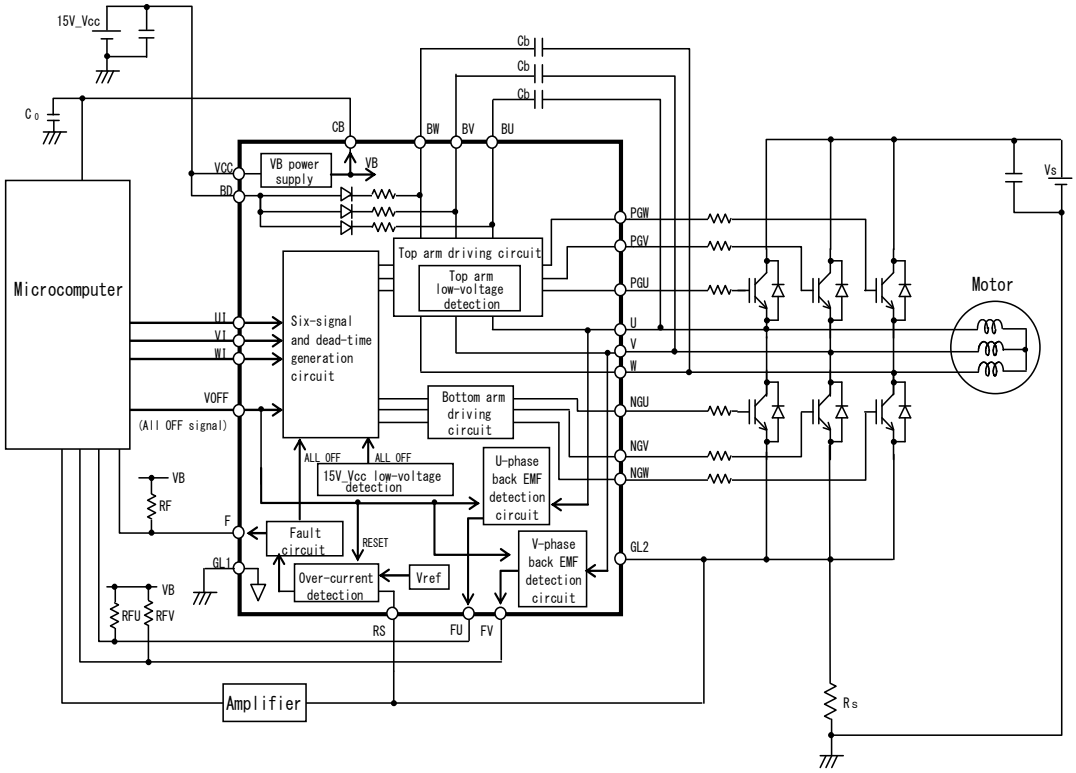


FIGURE 1.3.1 Block Diagram of ECN33550

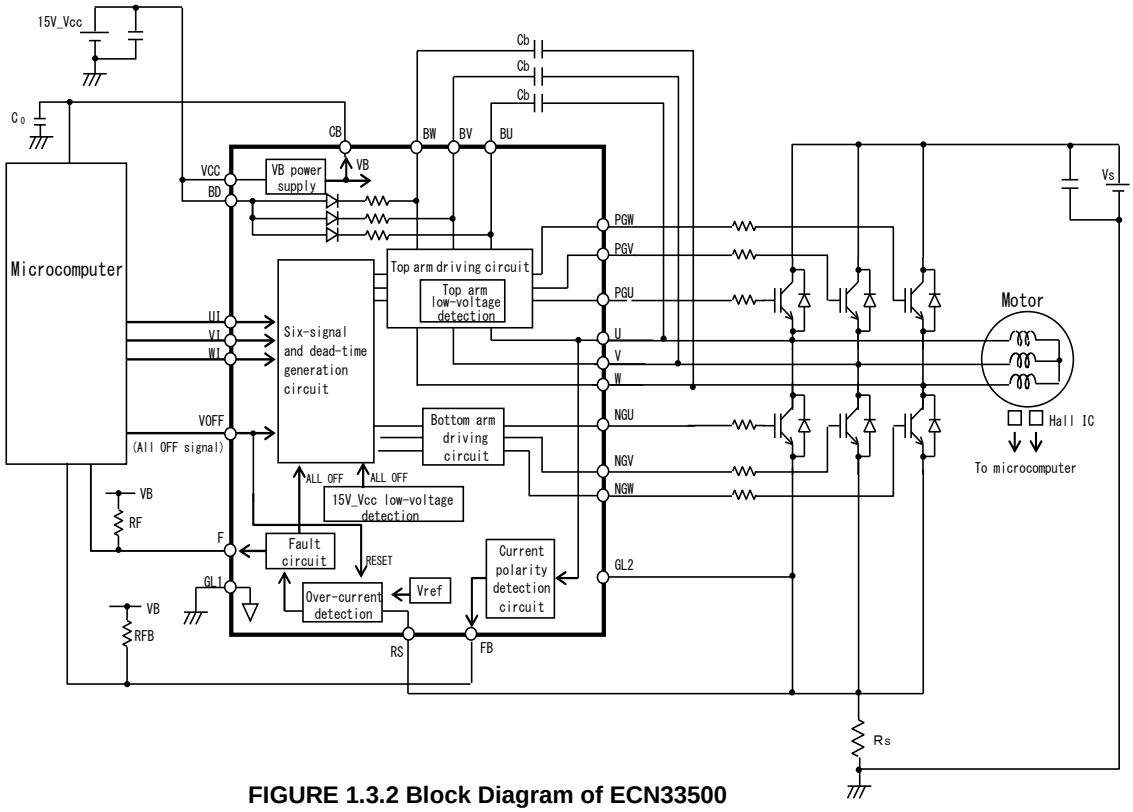


FIGURE 1.3.2 Block Diagram of ECN33500

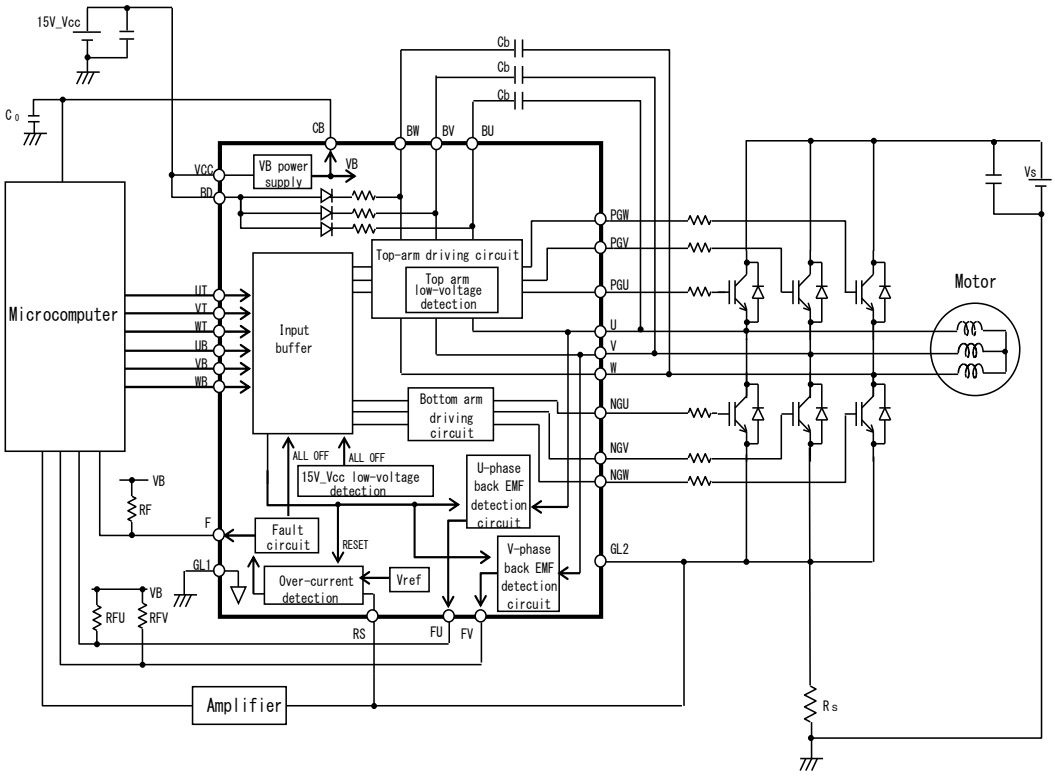


FIGURE 1.3.3 Block Diagram of ECN30551

2. Specifications

2.1 Pin Assignments

TABLE 2.1.1 shows the pin assignments.

TABLE 2.1.1 Pin Assignments

Pin	Pin names			Pin functions	Remarks
	33550	33500	30551		
1	WI		UT	WI: W-phase control signal input / UT: U-phase top arm control signal input	
2	VI		VT	VI: V-phase control signal input / VT: V-phase top arm control signal input	
3	UI		WT	UI: U-phase control signal input / WT: W-phase top arm control signal input	
4	VOFF		UB	VOFF: All OFF control signal input UB: U-phase bottom arm control signal input	
5	N.C.		VB	N.C.: No connection / VB: V-phase bottom arm control signal input	
6	N.C.		WB	N.C.: No connection / WB: W-phase bottom arm control signal input	
7	F			Fault signal output	
8	FU	FB	FU	FU: U-phase back EMF signal output FB: Current polarity signal output	
9	FV	N.C.	FV	FV: V-phase back EMF signal output / N.C.: No connection	
10	RS			Rs voltage input for over-current detection	
11	CB			VB power supply output	
12	GL1			Control system GND	
13	BD			For bootstrap diode	
14	VCC			15V control power supply	
15	GL2			Reference pin of bottom arm outputs (connected to a current detection resistor)	
16	NGW			W-phase bottom arm gate drive signal output	
17	NGV			V-phase bottom arm gate drive signal output	
18	NGU			U-phase bottom arm gate drive signal output	
19	W			Reference pin of W-phase top arm output	NOTE 1
20	BW			W-phase top arm driving circuit power supply	NOTE 1
21	PGW			W-phase top arm gate drive signal output	NOTE 1
22	V			Reference pin of V-phase top arm output	NOTE 1
23	BV			V-phase top arm driving circuit power supply	NOTE 1
24	PGV			V-phase top arm gate drive signal output	NOTE 1
25	U			Reference pin of U-phase top arm output	NOTE 1
26	BU			U-phase top arm driving circuit power supply	NOTE 1
27	PGU			U-phase top arm gate drive signal output	NOTE 1
28	GDM			Non-usable pin (GND potential. Do not connect anything to this pin.)	

Note 1. High voltage pin.

2.2 Pin Function

TABLE 2.2.1 Pin Function (1/3) [Model：ECN33550/33500/30551]

No.	Pin signs	Items	Functions and cautions	Related items	Remarks
1	VCC	Control power supply pin	・Powers the driving circuits for the bottom arms and the built-in VB supply circuit, etc. ・Determine the capacity of the power supply for 15V_Vcc, allowing for a margin determined by adding the standby current ICC and the current taken out of the CB pin.	・2.3.1 (1) 15V_Vcc low-voltage detection ・2.4.5 Notes Regarding VCC Pin ・4.1 to 4.5 Gate driver IC destruction by external surge	
2	CB	Output pin for built-in VB power supply	・Outputs a voltage generated in the built-in VB power supply (typ. 5.0V). ・Provides power from the VB power supply to the internal circuit of the gate driver IC (input buffer, over-current protection, etc.). Can be used as a power supply for MCU, position sensor signals. ・Connect oscillation prevention capacitor C0 to the CB pin. A capacitor capacity of 1.0μF ±20% is recommended.	・2.3.7 VB Power Supply	
3	GL1	Control GND pin	・The GND pin for the 15V_Vcc and VB power lines.		
4	GL2	Reference pin of bottom arm outputs	・Potential at this pin is reference potential of bottom arm outputs. ・Connected to shunt resistor Rs, it monitors phase current and over-current condition.	・2.3.1 (2) Over-current protection operation	
5	RS	Over-current protection detection signal input pin	・Detects over current condition. When the voltage at the RS pin exceeds the Vref (typ. 0.5V) the top and bottom arm outputs are all turned off.	・2.3.1 (2) Over-current protection operation	
6	U V W	Top arm output reference pin	・Reference potentials of each phase top arm output. ・Connect these pins to outputs of each phase bridge circuit and motor coils.	—	High voltage pin
7	BU BV BW	Top arm driving circuit power supply pin	・Powers the driving circuits for the top arms. ・Set the capacity of the bootstrap capacitor to an adequate value, allowing for charge current to the gate and switching conditions, etc.	・2.3.1 (1) Top arm power supply low-voltage detection ・2.3.2 Bootstrap Power Supply	High voltage pin
8	BD	Bootstrap diode pin	・Connected to phase top arm driving circuit power supplies (BU, BV, BW) respectively through high voltage diodes and current limiting resistors. ・Can be used for bootstrap by connecting to 15V_Vcc.	・2.3.2 Bootstrap Power Supply	
9	PGU PGV PGW	Top arm gate drive signal output pin	・Outputs gate drive signals for top arm output power devices of three-phase bridge circuit. ・Outputs BU, BV, BW voltage based on the U, V, W pin potential in each phase.	・2.4.1 Output Wiring ・2.4.4 Large Capacity of Output Power Device	High voltage pin
10	NGU NGV NGW	Bottom arm gate drive signal output pin	・Outputs gate drive signal for bottom arm output power devices of three-phase bridge circuit. ・Outputs 15V_Vcc voltage based on the GL2 pin potential.	・2.4.1 Output Wiring ・2.4.4 Large Capacity of Output Power Device	

TABLE 2.2.1 Pin Function (2/3) [Model：ECN33550/33500/30551]

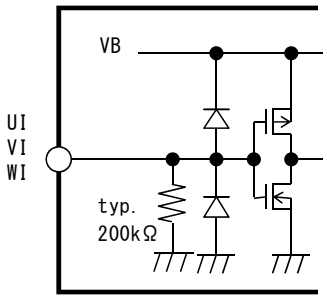
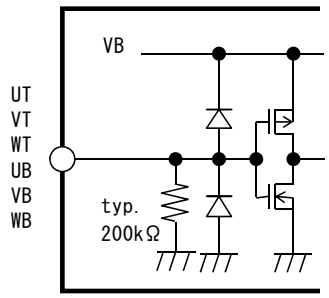
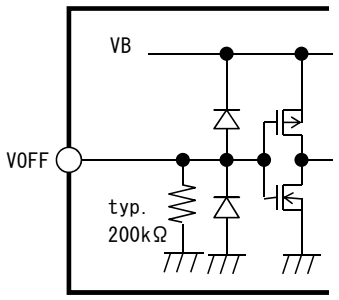
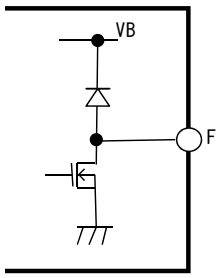
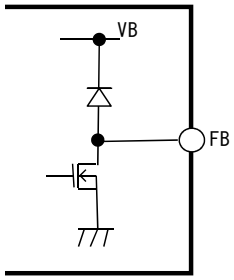
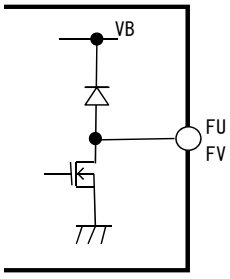
No.	Pin Signs	Items	Applicable model	Functions and cautions	Related items	Remarks
11	UI VI WI	Control signal input pin of each arm	ECN33550 ECN33500	・Inputs control signals of each phase. ・When inputting “H”, the top arm output becomes “H”. When inputting “L”, the bottom arm output becomes “H”. ・If the switching noise is monitored, mount a capacitor. ・The maximum rating of input voltage is VB+0.5V.	・2.4.2 Notes Regarding Input Pins	
						
		FIGURE 2.2.1 Equivalent Circuit around UI, VI, WI Pins				
12	UT VT WT UB VB WB	Control signal input pin of each arm	ECN30551	・Inputs control signals of each arm. The UT, VT, WT correspond to the top arm outputs. The UB, VB, WB correspond to bottom arm outputs. ・Input/output relation is ”H” active. ・If the switching noise is monitored, mount a capacitor. ・The maximum rating of input voltage is VB+0.5V.	・2.4.2 Notes Regarding Input pins	
						
		FIGURE 2.2.2 Equivalent Circuit around UT, VT, WT, UB, VB, WB Pins				
13	VOFF	All OFF control signal input pin	ECN33550 ECN33500	・When inputting “H”, H or L is outputted in accordance with the input control signal of each arm. ・When inputting “L”, the top and bottom arm outputs become “L”.	・2.4.2 Notes Regarding Input pins	
						
		FIGURE 2.2.3 Equivalent Circuit around VOFF Pin				

TABLE 2.2.1 Pin Function (3/3) [Model：ECN33550/33500/30551]

No.	Pin Signs	Items	Applicable model	Functions and cautions	Related items	Remarks
14	F	Fault signal output pin	ECN33550 ECN33500 ECN30551	・NMOS open drain output pin. Pull up to the CB pin or 5V through an external resistor RF (10kΩ±5% recommended). ・Outputs “L” when the over-current protection operates. ・Outputs “H” in a normal state.	・2.3.1 (2) Over-current protection operation	
						
		FIGURE 2.2.4 Equivalent Circuit around F Pin				
15	FB	FB signal output pin	ECN33500	・NMOS open drain output pin. Pull up to the CB pin or 5V through an external resistor RF (10kΩ±5% recommended). ・Outputs U-phase motor current polarity signal. ・Outputs “L” when the motor current polarity is “negative”. Outputs “H” when the motor current polarity is “positive".	・2.3.6 Current Polarity Detection Function	
						
		FIGURE 2.2.5 Equivalent Circuit around FB Pin				
16	FU FV	FU/FV signal output pin	ECN33550 ECN30551	・NMOS open drain output pin. Pull up to the CB pin or 5V through an external resistor RF (10kΩ±5% recommended). ・Outputs U-phase and V-phase back EMF signal while the inverter stops the operation (33550: VOFF=L 30551: UB, VB, WB, UT, VT, WT=L). ・Outputs “H” when the U or V pin voltage is the VIH or higher. Outputs “L” when the U or V pin voltage is the VIL or lower.	・2.3.5 Back EMF Detection Function	
						
		FIGURE 2.2.6 Equivalent Circuit around FU, FV Pins				

2.3 Functions and Precautions

2.3.1 Protection Function

(1) Low-voltage detection

(a)15V_Vcc low-voltage detection

Hitachi Power Semiconductor Device calls the 15V_Vcc low-voltage detection “LVSD”. When the 15V_Vcc voltage goes below the LVSD operating voltage (LVSDON), the gate driver IC outputs of the top and bottom arms are all turned off regardless of the input signals. This function has hysteresis (Vrh). When the 15V_Vcc voltage goes up again, the system returns to a state in which the gate driver IC output operates according to the input signals, at a level equal to or exceeding the LVSD recovery voltage (LVSDOFF).

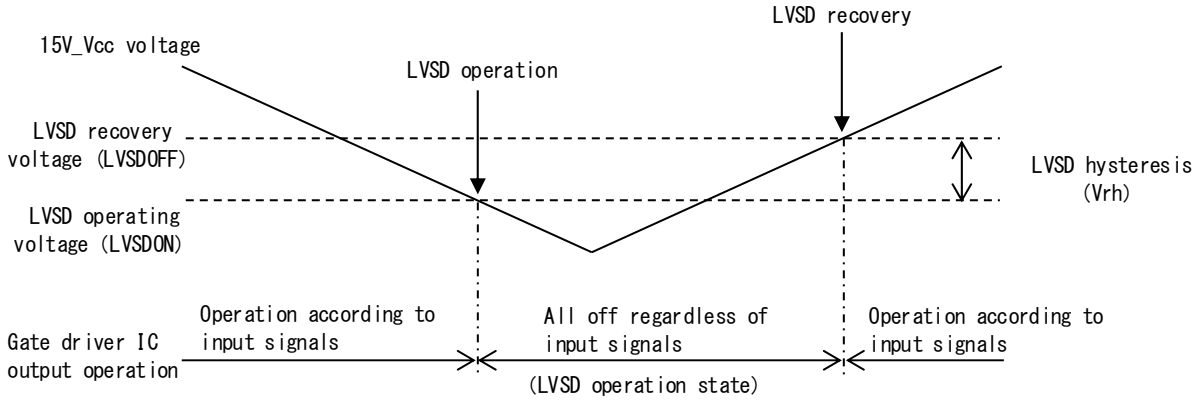


FIGURE 2.3.1.1 Timing Chart for 15V_Vcc Low-voltage Detection (LVSD Operation)

(b) Top arm power supply low-voltage detection

When the top arm power supply voltages (voltages between BU and U, BV and V, BW and W) goes below the top arm LVSD operating voltage (LVSDONT), top arm output of the corresponding phase becomes “L” even when the top arm input signals are “H”. This function has hysteresis (Vrh). The “L” output state is reset when the “H” signal is input to the top arm after the top arm power supply voltages go up to the top arm low-voltage detection recovery voltage (LVSDOFFT). When the “L” output state is reset in a state in which the top arm input signal is “H”, the top arm is not turned on. This is because of latch function of top arm driving circuit (see Section 2.3.8 Level Shift Circuit). By inputting the ”L” signal and then inputting the “H” signal again, the top arm is turned on.

(c) Notice

If the 15V_Vcc low-voltage detection or the top arm power supply low-voltage detection operates during motor rotation, Vs voltage may rise due to regenerative electric power. The Vs voltage must not exceed the maximum rating of the output power device. Particular attention is needed when the capacity between the Vs and GND is small, making the voltage more likely to rise.

(2) Over-current protection

(a) Over-current protection operation

These ICs detect the current using the voltage at the RS pin. When the voltage at the RS pin exceeds the Vref (typ. 0.5V) of the internal detection circuit, the gate driver IC output of the top and bottom arms are all turned off and the F pin output is “L”.

After the over-current protection operates, the reset method is as follows:

① ECN33550/ECN33500：Input “L” to the VOFF pin

② ECN30551：Input “L” to all of the UT, VT, WT, UB, VB and WB pins

By inputting “L” as described in ① or ②, the F pin output become “H” after the Fault reset delay time (tflrs) passes. The period to input “L” as described in ① or ② must be longer than the Fault reset delay time.

The IC may turn to a state in which the over-current protection operates after the 15V_Vcc power-on. In this case, reset the IC.

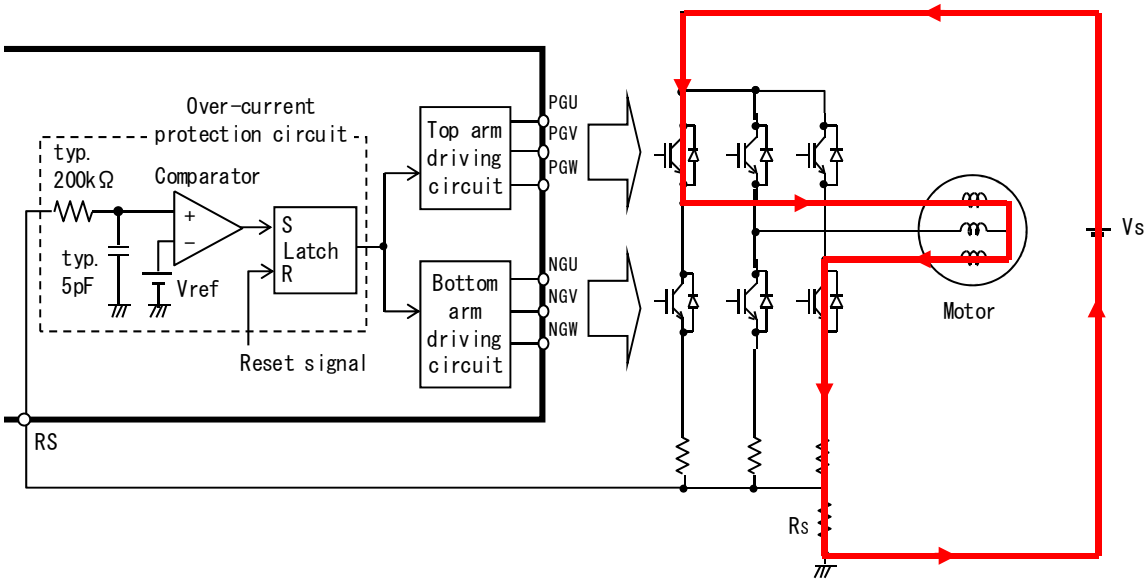


FIGURE 2.3.1.2 Example of Current through Shunt Resistance

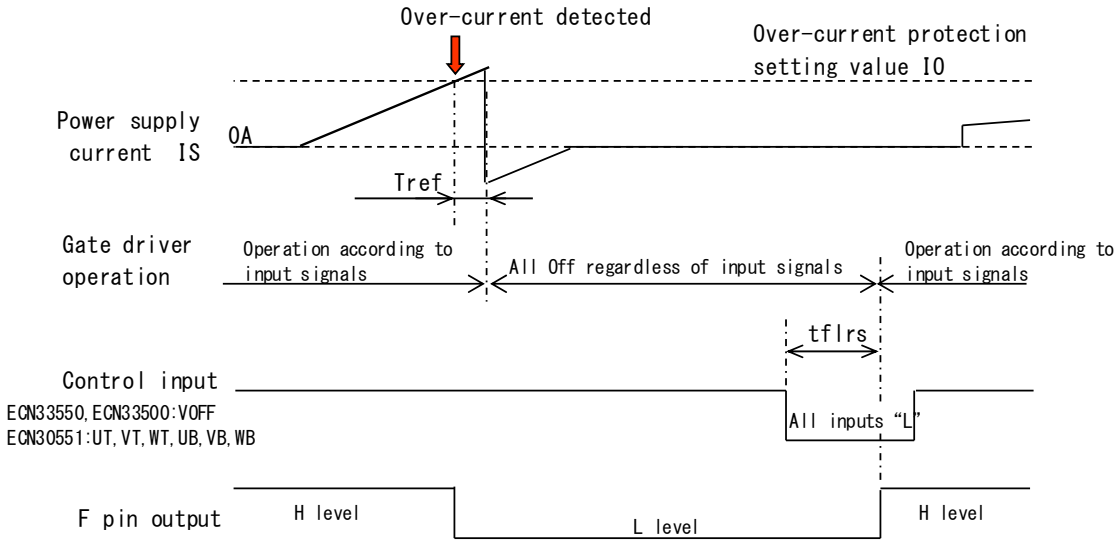


FIGURE 2.3.1.3 Timing Chart of Over-current Protection Operation

(b) How to set up over-current protection level

The over-current protection setting I0 is calculated as follows;

IO=Vref/Rs

where

Vref: Reference voltage for current protection

Rs : Resistance of shunt resistor

In setting an over-current protection level, you should allow for Vref variance, Rs variance, and the delay from the time the over-current protection operates until the time the output power device is turned off. In practice, check the coil current of the motor.

Set the shunt resistance so that voltage of the GL2 pin is within the specified GL2 allowable voltage (VGL2) range. This function is not effective for currents that do not flow forward (direction to the GL pin) through the shunt resistor, such as reflux current and power regenerative current (see Figures. 2.3.1.4 and 2.3.1.5).

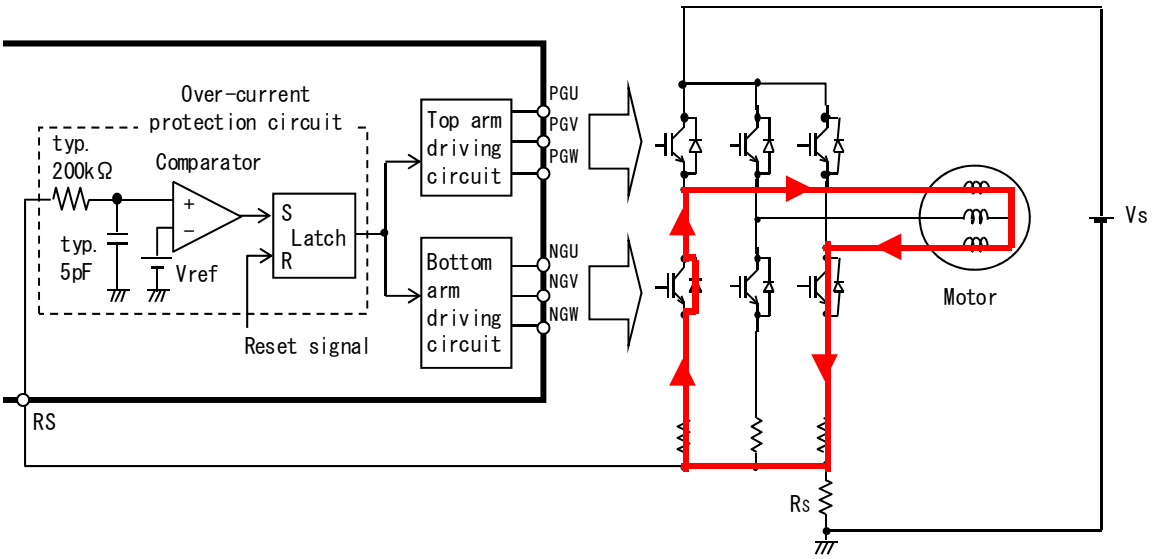


FIGURE 2.3.1.4 Example of Reflux Current

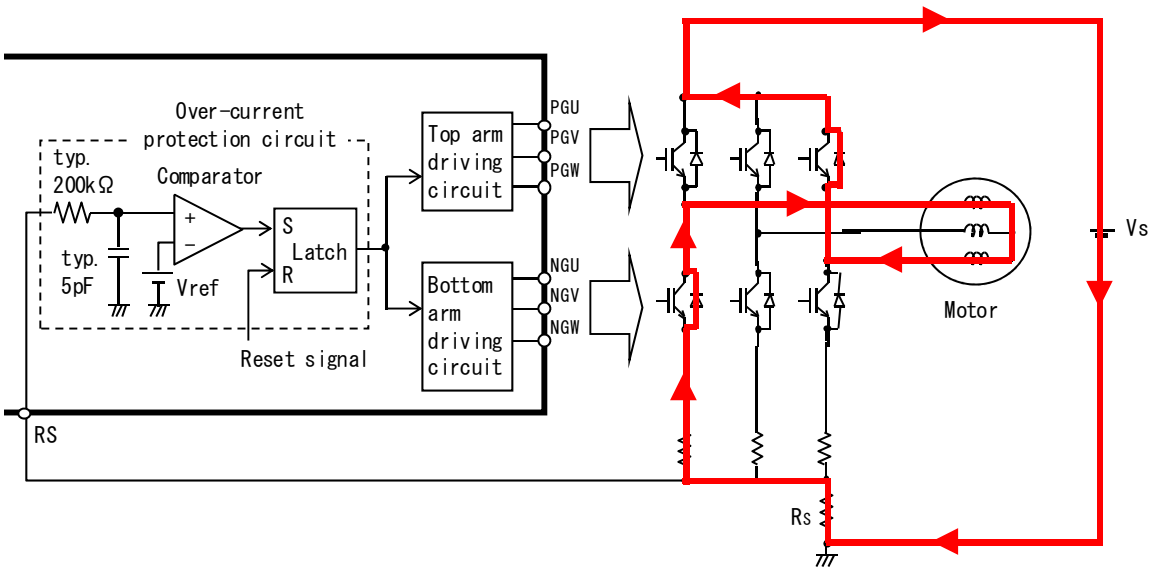


FIGURE 2.3.1.5 Example of Power Regenerative Current

(c) Precautions

・Shunt resistor Rs

Minimize the inductance of wiring of the shunt resistor Rs as far as possible (see Fig. 2.3.1.6). If the wiring has a high resistance or inductance, the emitter potential of the bottom arm IGBTs (source potential of MOS) changes, which can result in IGBT (MOS) malfunction.

When the over-current protection operates, minus surge voltage (Va) may be generated in the shunt resistor Rs by this inductance (Ls) and the di/dt of current. This minus surge voltage (Va) is applied between the GL1 pin and each of the GL2 pin, the bottom arm output pins NGU, NGV and NGW (through MOS/IGBT gate capacity coupling). This may destroy the IC in the worst case. This minus surge voltage (Va) must not exceed −5V between the GL1 pin and each of the GL2, NGU, NGV, and NGW pins. To suppress this minus surge voltage, effective measures are:

① to make the wiring of the shunt resistor Rs as short as possible,

② to use a non inductive shunt resistor, and

③ to clamp a surge voltage by adding the diode Ds in reversely parallel to the shunt resistor.

In this case, be aware that the effects depend on a connecting point and specification of a diode to be selected.

It is recommended to use a fast recovery diode. Select its rating in according to a motor current.

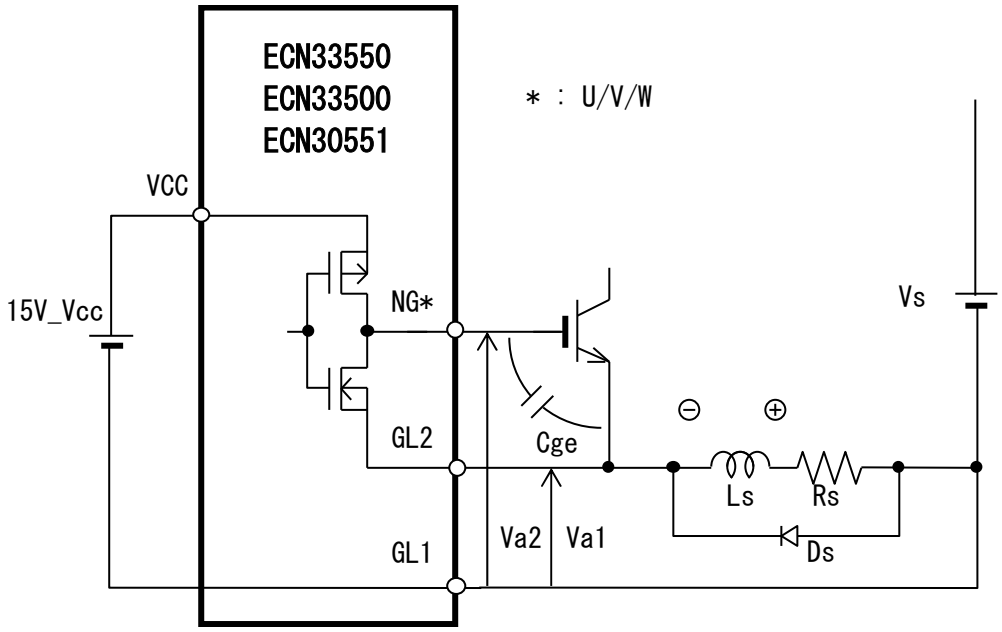


FIGURE 2.3.1.6 Over-voltage Generation around Shunt Resistor

・Noise in RS pin

The RS pin incorporates a CR filter having a time constant of about 1μs. If the over-current protection malfunctions, it is effective to add a CR filter externally. However, be aware that the delay from the time the over-current state occurs until the over-current protection operates becomes longer by adding an external CR filter.

2.3.2 Bootstrap Power Supply

(1) Outline of bootstrap power supply

A bootstrap system is a power supply method to the top arm driving circuit. By charging an external capacitor Cb, potential higher than the Vs is obtained. Each negative side pin of the capacitors Cb is connected to a midpoint of each phase bridge circuit (the U, V, W pins), and each positive side pin is connected to the top arm power supply pin of each phase (BU, BV, BW).

Fig. 2.3.2.1 shows the simplified circuit diagram of the bootstrap power supply for the top arm driving circuit. When the output power devices of the bottom arms are turned on, the capacitor Cb is charged (through passage ①). The output power device on-duty is limited because this charge in the capacitor Cb is consumed as a power supply for the top arm driving circuit. Bootstrap system is more superior in terms of cost compared to floating power supply as a power supply for the top arm driving circuit. However, it is necessary to charge the capacitor at an initial state in order to drive the top arm driving circuit.

The ON duration of the top arm output power device is affected by the capacitance of the capacitor Cb. Particular attention is needed when PWM carrier frequency is low.

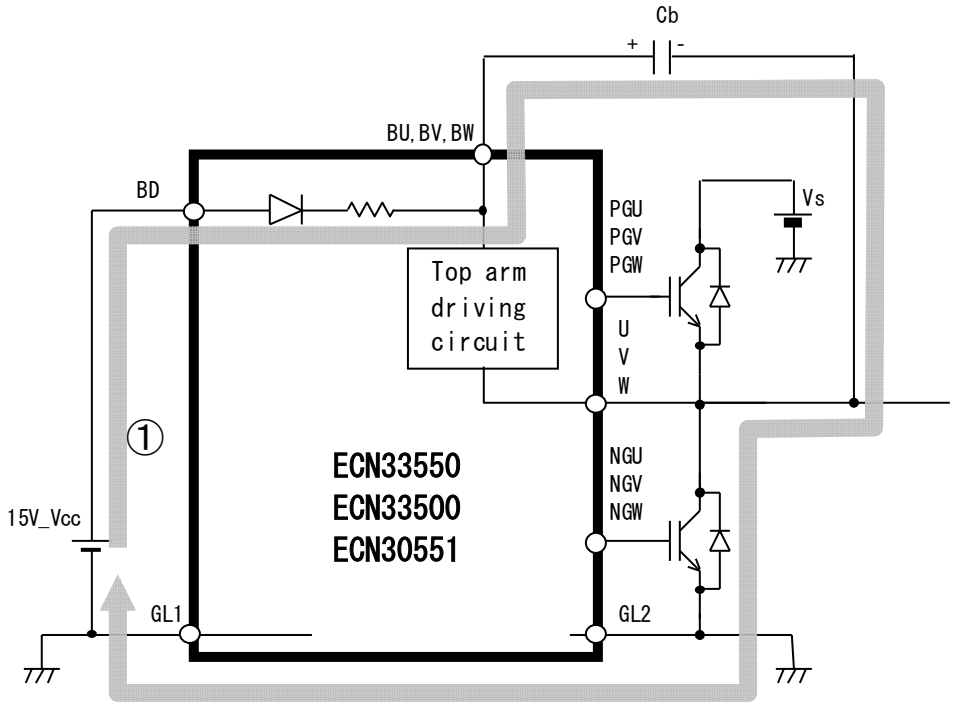


FIGURE 2.3.2.1 Bootstrap Power Supply

(2) Built-in bootstrap diode and current limiting resistor (BD pin)

As shown in figures 1.3.1, 1.3.2 and 1.3.3, the gate driver ICs incorporate high voltage diodes for bootstrap and current limiting resistors between the BD pin and each of the BU, BV, BW pins. Each resistance Rbd between the BD pin and each of the BU, BV, BW pins is about 180Ω. The voltage of the bootstrap capacitor Cb depends on the resistance Rbd, the on-duty of the output power device, and the capacitance of the capacitor Cb. Set the capacitance of the capacitor Cb and the on-duty in consideration of use conditions and use environment such that the bootstrap voltage does not go down to the maximum value of the top arm LVSD operating voltage (12.0V) or below while the inverter operates. (See the following subsection (3).)

It is also possible to mount the high voltage diode and the current limiting resistor as external parts between the 15V_Vcc power supply and each of the BU, BV, BW pins without using the built-in bootstrap diodes and current limiting resistors. In this case, the BD pin must be held at a GND potential.

(3) Bootstrap circuit parts

(a) Bootstrap capacitor Cb

・Mount the Cb as close to the IC as possible to prevent the IC from being destroyed by over-voltage.

・An optimal capacity value of the bootstrap capacitor Cb varies depending on switching frequency, an on-duty of the output power device and a gate capacity.

・During the period from one charge to the next charge of the Cb, the top arm power supply voltage gradually goes down, because the charge accumulated in the capacitor Cb is consumed by a leakage current of the top arm driving circuit and the gate charge current of the top arm output power device. When the top arm power supply voltage goes down to the top arm low-voltage operating voltage, the top arm output is turned off. Therefore, the capacity value of the capacitor Cb is an important factor to prolong an ON-time of the top arms. The period from charging the Cb until the top arm is turned off is “tOnMax”. This can be calculated using the following formula:

$$tOnMax = \{(VCb - LVSDONT) \times Cb - Q1 \times n\} / Is2$$

VCb：Top arm power supply voltage after charging bootstrap
LVSDONT：Top arm low-voltage operating voltage
Cb：Capacitance of bootstrap capacitor
Q1：Electric charge charged in output power device gate (@VCb)
n：The number of operation of top arm output power device
Is2：Leakage current of the top arm driving circuit

Select the capacitance Cb of the bootstrap capacitor in accordance with the top arm maximum ON-time (tOnMax) and electric charge required for charging the output power device gates Q1. For reference, the calculated examples are shown below when VCb=15V, LVSDONT=12V, n=1 (once), Is2=30μs.

Example of output power device (Renesas Electronics type)	Gate charge Q1 (μC)	Cb (μF)	Top arm maximum ON-time tOnMax (ms)
600V/10A MOS (RJK6012DPP-E0)	0.040	1.0	99
600V/35A IGBT (RJH60M3DPP-M0)	0.060	1.0	98
600V/35A IGBT (RJH60M3DPP-M0)	0.060	3.3	328
600V/35A IGBT (RJH60M3DPP-M0)	0.060	5.6	558

When adding a capacitor between the output pin of the IC and the output power device as shown in Fig. 2.4.1.1, consider a capacitance of the capacitor added.

When the number of operation of the top arm output power device is $n \geqq 2$ (twice or more), the tOnMax becomes short because the larger the number of times of gate charging of the output power device is, the sooner the Cb is discharged. Under sine wave drive, the state will be generally “n=1” because the top and bottom arm output power devices operate alternately. However, when the PWM signal of the MCU and the operation of the output power device do not correspond, there is a possibility that “$n \geqq 2$” because either the top arm or bottom arm output power device operates. For example, in the narrow pulse width region of the PWM signal, this correspondence between the MCU PWM signal and the output power device operation is affected by the internal filter function of the gate driver IC (removing pulse having narrow pulse width in an input signal) and operation delays of the gate driver IC and the output power device. For this reason, it is estimated that the MCU PWM signal and the output power device operation do not correspond. When evaluating your system, a care (for example, check an on-duty and bootstrap voltage with actual output power device and select optimal capacitors Cb) is needed.

(b) Bootstrap current limiting resistor：Rb (When using external parts)

The Rb is important to limit the Cb initial charging current (inrush current) during the bootstrap operation. Make sure to insert the Rb because large inrush current adversely affects the system as described below.

① Destruction of bootstrap diode Db caused by surge current

Set the Rb to suppress the surge current below the allowable surge current value of the diode.

② Malfunction of over-current protection

The Cb inrush current flows through the bottom arm output power device to the shunt resistor for over-current detection. When this current exceeds the over-current detection level, the IC performs the over-current protection. Adjust the Rb to suppress the inrush current below the over-current detection level.

③ Destruction of top arm driving circuit caused by over-voltage

If the inrush current is large, over-voltage is generated during switching operations of the output power device under the influence of wiring reactance, which may result in gate driver IC destruction. Restrain the inrush current and take measures such as mounting the capacitor Cb close to the IC so as not to cause over-voltage.

(c) Bootstrap diode：Db (When using external parts)

Recommended diode Db is: Withstand voltage = 600V or more
Forward voltage = sufficiently small
Reverse recovery time trr = 100ns or less

If the forward voltage is large, the top arm power supply voltage drops. If trr is large, the Db reverse recovery current Irr flows into the 15V_Vcc power supply when the top arm output power device is turned on. This decreases efficiency of the bootstrap power supply.

The followings are recommended as a standard application. However, determine your application by evaluating your system.

Db：Hitachi fast diode DFG1C6 (glass mold) or DFM1F6 (resin mold)
Cb：3.3μF±20%【stress voltage：15V_Vcc】
Rb：3.3Ω±20%【2W or more】

2.3.3 Dead Time

・Each phase has two output power devices, which have a totem pole configuration. If the top and bottom arm of the same phase are simultaneously turned on, short-circuit current flows. This may destroy the output power devices and a gate driver IC. Therefore, when the output control is shifted from top arm (bottom arm) OFF to bottom arm (top arm) ON in the same phase, it is necessary to secure the period the top and bottom arms in the same phase are OFF (dead time).

・For three-input type (ECN33550/ECN33500), in the IC, the top and bottom arm signals of each phase are generated from one input signal after the dead time is added to them. Therefore, the top and bottom arms do not output ON signals simultaneously in principle of operation. However, these are the outputs of the gate driver IC, not output power devices. It is necessary to secure a dead time for the output power devices. In consideration of the delay time of the output power device operation, be careful when setting the gate resistance and gate capacity such that the top and bottom arm outputs are never ON simultaneously in any case.

・The six-input type (ECN30551) incorporates a logic circuit capable of prohibiting the top and bottom arms from outputting the ON signals simultaneously. (A dead time is not generated.) This circuit works based on only the input signals, and does not work for delays of the gate driver IC output nor the output power device operation. Set a dead time to the input signals such that the top and bottom arm outputs of the output power devices are never ON simultaneously in any case.

2.3.4 Internal Filter Circuit

Internal filter circuits are located before the top and bottom arm driving circuits in these gate driver ICs (ECN33550/33500/30551). The filter circuits remove switching noise and narrow pulse signals inputted to the control signal input pins of each arm of the gate driver IC (ECN33550/33500:UI,VI,WI. ECN30551:UT,VT,WT,UB,VB,WB). As a guide, pulse width removed by the filter circuits is equal to or shorter than the turn-on/off output delay time of each phase.

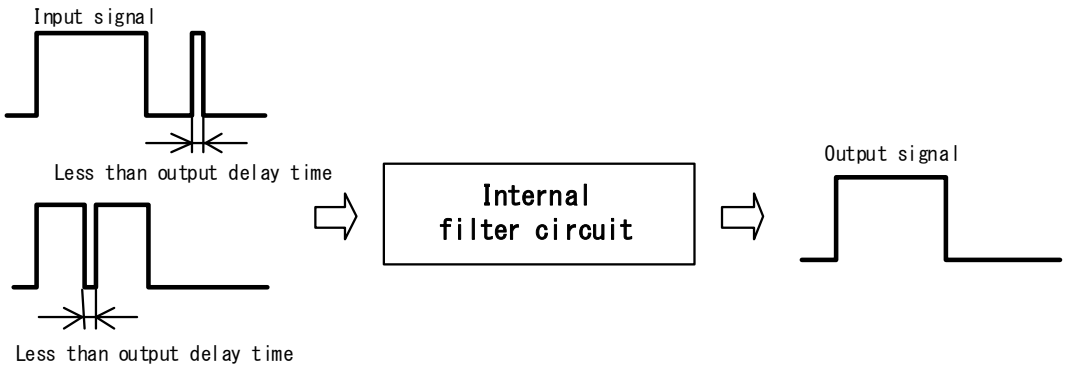


FIGURE 2.3.4.1 Example of Internal Filter Circuit Operation

2.3.5 Back EMF Detection Function (Model：ECN33550, ECN30551)

・When the motor is rotated by external force (free run) during stop of the inverter operation, the FU pin and FV pin output the U-phase back EMF signal and V-phase back EMF signal respectively as rotor position information. The condition which the gate driver IC outputs the back EMF signals is satisfied when:

ECN33550：the VOFF pin input is “L”

ECN30551：the inputs of the UB, VB, WB, UT, VT and WT pins are all “L”

Under conditions other than the above, the FU and FV signals cannot be used as the rotor position information.

2.3.6 Current Polarity Detection Function (Model：ECN33500)

・The FB pin outputs the U-phase current polarity signal as the phase information of the motor current while the inverter is operating. Regarding the motor current polarity, it is assumed that the direction from the output power device side to the motor coil side is set to positive, the direction from the motor coil side to the output power device side is set to negative. When the motor current polarity is “positive”, the FB pin outputs “H”. When the motor current polarity is “negative”, the FB pin outputs “L”.

・Whether the current polarity signal is “H” or “L” is detected from the information on U-phase voltage using a latch circuit. This latch circuit is triggered by the output of the gate driver IC. Therefore, when a time after the gate driver IC outputs a gate drive signal until the output power device operates is too long, there is a possibility that current polarity signal information cannot be detected accurately.

When the current polarity is “negative”, the time after the bottom arm of the gate driver IC outputs “L” until the U-phase output voltage becomes “H”, this time is set to “tdpoffB”. (Fig. 2.3.6.1 shows the definition of the tdpoffB.) To detect the current polarity signal information accurately, select your output power device and set the gate resistance and capacity such that the tdpoffB is less than or equal to 0.7μs while considering variance and temperature dependence.

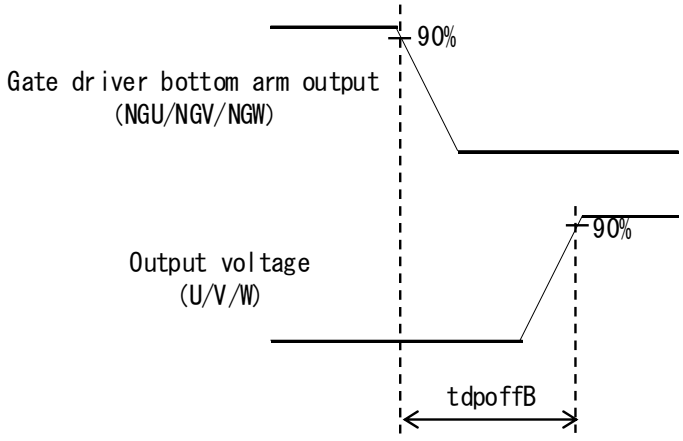


FIGURE 2.3.6.1 Definition of tdpoffB

2.3.7 VB Power Supply

The VB power supply (VB = typ. 5.0V) to be output to the CB pin is generated from 15V_Vcc power supply. The VB power is supplied to the internal circuits of the IC such as the over-current protection circuit.

The VB power supply circuit constitutes a feedback circuit (see Fig. 2.3.7.1). To prevent oscillation, connect a capacitor C0 to the CB pin.

The recommended capacity for the C0 is 1.0μF±20%.

The larger the C0 capacity, the more stable the VB power supply. However, a too large C0 capacity causes the operation delay of the VB power supply in the IC at a transient time such as the power supply sequence. Setting the capacity figure to an excessive level is not recommended. As a guide, it should be 3μF or less. Input the control inputs after the VB power supply is sufficiently stable.

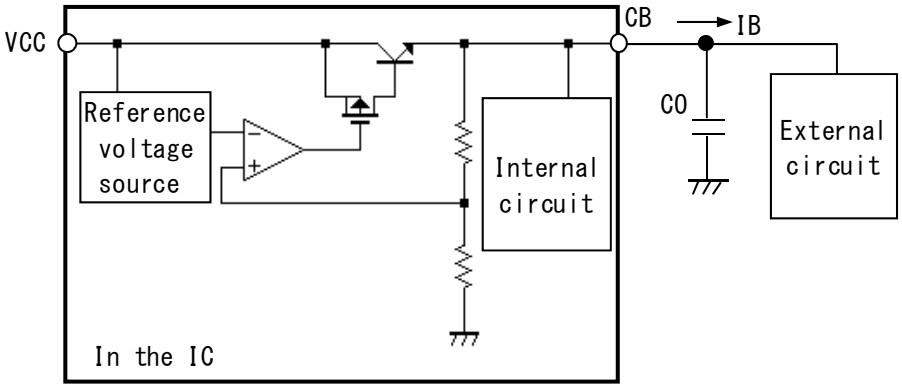


FIGURE 2.3.7.1 VB Power Supply Equivalent Circuit

2.3.8 Level Shift Circuit

Fig. 2.3.8.1 shows the level shift circuit configuration. The level shift circuit converts the input signal based on GND level into the top arm gate drive signals based on the U, V, W voltage of each phase at floating potential. The driving circuit of the high voltage NMOSes (a) and (b) for level shift uses a latch circuit that is triggered at rising edges of the input signals in order to reduce the current consumption of the level shift circuit.

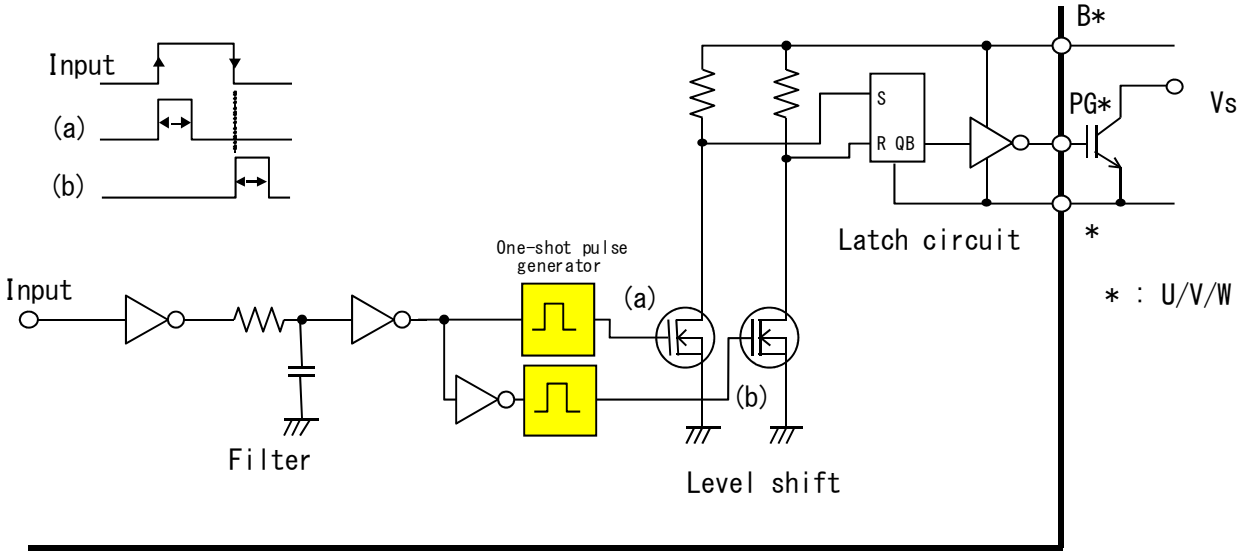


FIGURE 2.3.8.1 Configuration of Level Shift Circuit

2.4 Precautions for Use

2.4.1 Output Wiring

Make the wiring for connecting between the output pin of the gate driver IC and the output power device as short as possible in order to minimize the inductance. The output voltage of the gate driver IC is oscillated at the frequency determined based on the wire inductance Lw and the gate capacity Cg of the output power device. When this oscillation voltage exceeds the maximum rating of the IC (for example, for U-phase top arm output, the voltage between PGU and U is 20V. For U-phase bottom arm output, the voltage between NGU and GL2 is 20V.), the IC may be destroyed. Therefore, connect the following parts close to the top and bottom arm output pins of each phase of the IC as shown in Fig. 2.4.1.1.

・Capacitor CP (e.g. 560pF (In case of wiring length is about 30cm using a ceramic capacitor. Regulate the value depending on length.))

・Gate series resistor Rg (e.g. 100Ω (In case of IGBT 20A class. Regulate the value depending on current capacity of an external device.))

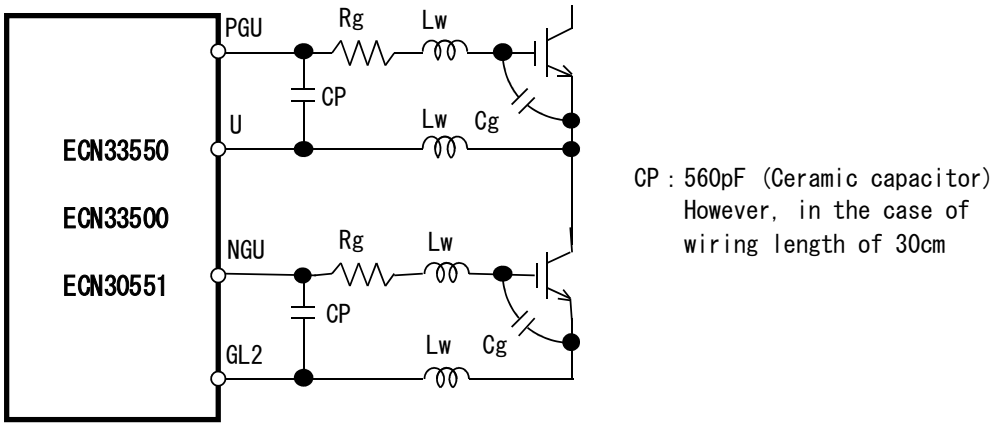


FIGURE 2.4.1.1 Addition of Capacitor CP for Preventing Oscillation (Only U-phase)

2.4.2 Notes Regarding Input Pins

The input pins (ECN33550/33500: UI, VI, WI, VOFF. ECN30551: UT, VT, WT, UB, VB, WB) operate at a CMOS logic level of the internal regulator voltage VB of the gate driver IC. If you use an external power supply for the MCU for control, be careful that the voltage of the input signal does not exceed the rating of the input pin (−0.5V to VB+0.5V) due to the fluctuations in the external power supply voltages.

These input pins are susceptible to the dv/dt noise in a switching operation of the output power device because they have large impedance. Therefore, when designing a printed circuit board (PCB), take anti-noise measures on a PCB such that switching noise of the output power device does not couple on the input pins. Any noise coupled on the pins will cause improper operation, overheat, and over-voltage of the IC, which could result in the IC destruction.

In particular, when using temporary wiring for evaluation, it is effective to insert the filter (shown in Fig. 2.4.2.1) onto the input pins against switching noise. In this case, regarding the six-input type, attention must be paid to risk of short circuits of the top and bottom arms, because the input pulses are delayed. (Regarding the three-input type, the input pulse delay does not cause short circuits of the top and bottom arms in principle.) Since a large current flows when a short circuit occurs, the ground line is oscillated, which could lead to over-voltage in the IC.

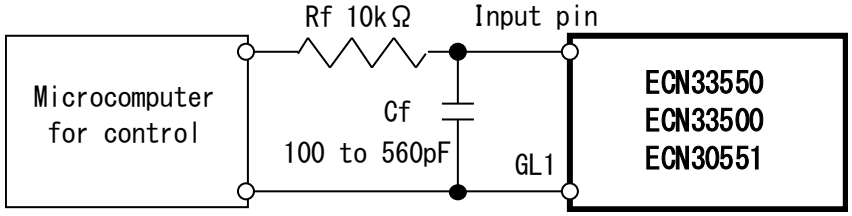


FIGURE 2.4.2.1 Insertion of Input Filter

2.4.3 Initial Setting in Turning on Power

When the 15V_Vcc power supply is turned on, set the following pins to be all OFF (ECN33550/33500：VOFF=L、ECN30551：UT,VT,WT,UB,VB,WB=L). After the 15V_Vcc power supply becomes stable, input the ON signal.

The top arm power supply voltage must be more than the top arm LVSD recovery voltage (LVSDOFFT). Therefore, it is necessary to initially charge the capacitor Cb before the inverter operation. The capacitor Cb is charged by turning on the bottom arm of the corresponding phase. The ON-time of bottom arm during initial charging is set based on the time constant calculated by multiplying Rbd by Cb (Rbd × Cb). The Rbd represents the resistance between the BD pin and each of the BU, BV, BW pins (when using an external component, the Rbd depends on characteristics of an external component). In general, as an initial setting after the power supply is turned on, it is recommended to input a bottom arm On-pulse width which is 3 times or more of T=Rbd × Cb.

2.4.4 Large Capacity of Output Power Device

In theory, the capacity of the output power device can be increased by connecting an external CMOS buffer to the output pin of the IC. However, when the capacity is increased, fast large current switching is likely to cause surge voltage and oscillation, and a possibility that could lead to malfunction or destruction of the gate driver IC becomes higher. Therefore, consider noise and over-voltage suppression before increasing the capacity of the output power device.

2.4.5 Notes Regarding VCC Pin

The VCC pin supplies output current, and whenever the output of the gate driver IC is turned on, the pulse current, whose peak is several hundred mA, flows. If there is wiring inductance in the VCC pin wiring, the noise of L×di/dt occurs at the VCC pin of the IC by the pulse current. When this noise exceeds the maximum rating of the 15V_Vcc, the IC may be destroyed. To avoid this, take measures to minimize the inductance. Connect the capacitor as close to the VCC pin as possible. It is effective to mount a plurality of ceramic capacitors (bypass capacitor) of several hundred pF to several uF connected in parallel with an electrolytic capacitor. As a guide, the capacity of the electrolytic capacitor should be 10 times or more of the bootstrap capacitor Cb.

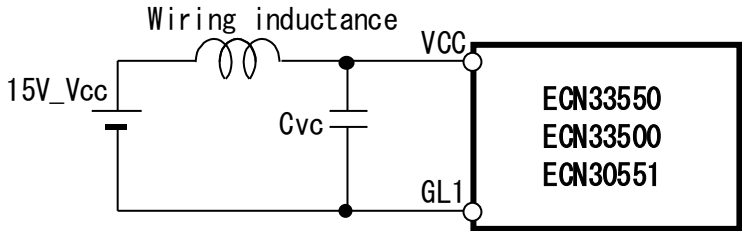


FIGURE 2.4.5.1 Addition of Capacitor for 15V_Vcc Power Supply

2.4.6 Others

See “Instructions for Use of Hitachi High-Voltage Monolithic ICs” for other precautions and instructions on how to deal with these products.

2.5 Power Consumption and Temperature Rise

2.5.1 Power Consumption

The power consumption of these ICs is classified roughly into following three items.

(1) Power required for charging/discharging of gate capacity of external output power devices
(2) Power consumption in high voltage circuits (level shifting circuits) in the IC
(3) Power consumption in control circuit (15V_Vcc power system circuit) in the IC

Fig. 2.5.1 shows the example of the power consumption calculated under the following conditions.

Gate capacity of an output power device：C = 1000pF
Control power supply voltage：15V_Vcc = 15V
High voltage power supply voltage：Vs = 280V
PWM frequency：f_{PWM} = 1 to 30kHz

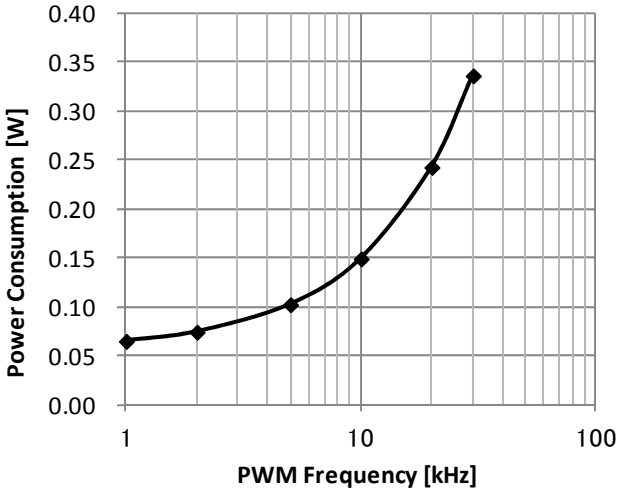


FIGURE 2.5.1 Calculation Example of Frequency-dependency of Power Consumption

2.5.2 Temperature Rise

A calculation example of temperature rise from the power consumption when the PWM frequency is 20kHz is shown below (power consumption, about 0.24W). When the PCB specifications for mounting is “PCB material: glass epoxy, size: 40mm×40mm×1.6mm, wiring density: 10%”, the thermal resistance of the gate driver IC package is 96℃/W (reference value). The temperature rise δT can be calculated using the following formula:

$$\delta T = 0.24\ (W) \times 96\ (℃/W) = 23\ (℃)$$

2.6 Mounting

(1) Insulation between pins

High voltages are applied between the pin numbers specified below. Apply coating or mold (for all ECN33550/ ECN33500/ECN30551).

Between pin numbers：18-19, 21-22, 24-25, 27-28

There are many kinds of coating resins. It is unclear what kind of influence of coating resin has on semiconductor devices (thermal stress, mechanical stress and other stress) by PCB size, shape, thickness, and mounting parts to be used. When selecting a coating resin, consult with your PCB manufacturer.

(2) Precautions for N.C. Pin Wiring

All of the N.C. pins are not connected to the IC (chip). Therefore, the withstand voltage is more than 600V. However, they constitute part of parasitic capacity of the ICs. The capacity value between the pins are tens of pF or thereabouts. When connecting the wiring to the N.C. pins, design a PCB while taking this parasitic capacity into account.

2.7 Markings

The resin surface of the IC is marked by laser.

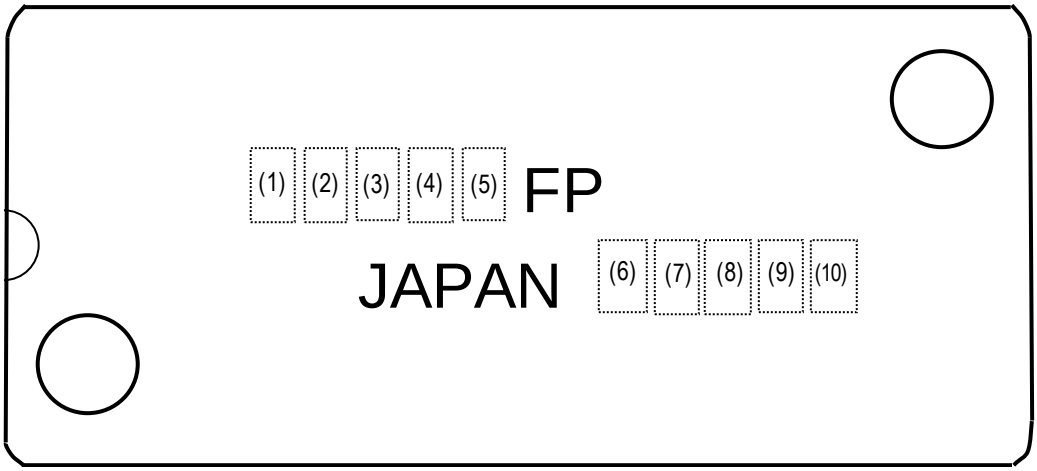


FIGURE 2.7.1 Marking Specifications

Mark No. (1) to (5): Model name

Mark No. (6) to (10): Lot number

No. (6)：Last one-digit of the year of assembly

No. (7)：Month of assembly:

January: A, February: B, March: C, April: D, May: E, June: K,

July: L, August: M, September: N, October: X, November: Y, December: Z

No. (8) to (10)：Quality control number

Represented with letters from “A” to “Z” except “I” and “O”, numbers from “0” to “9”, or blank.

3. Recommended Circuit

3.1 Standard External Parts

Figures 3.1.1, 3.1.2 and 3.1.3 show examples of recommended circuits. These are just indicators. Select peripheral parts considering redundancy in design.

Select parts based on specific user situations. To absorb voltage surges, mount each part close to the IC pins. Make the wiring between the shunt resistor Rs and the RS pin and between the RS pin and the GL2 pins as short as possible.

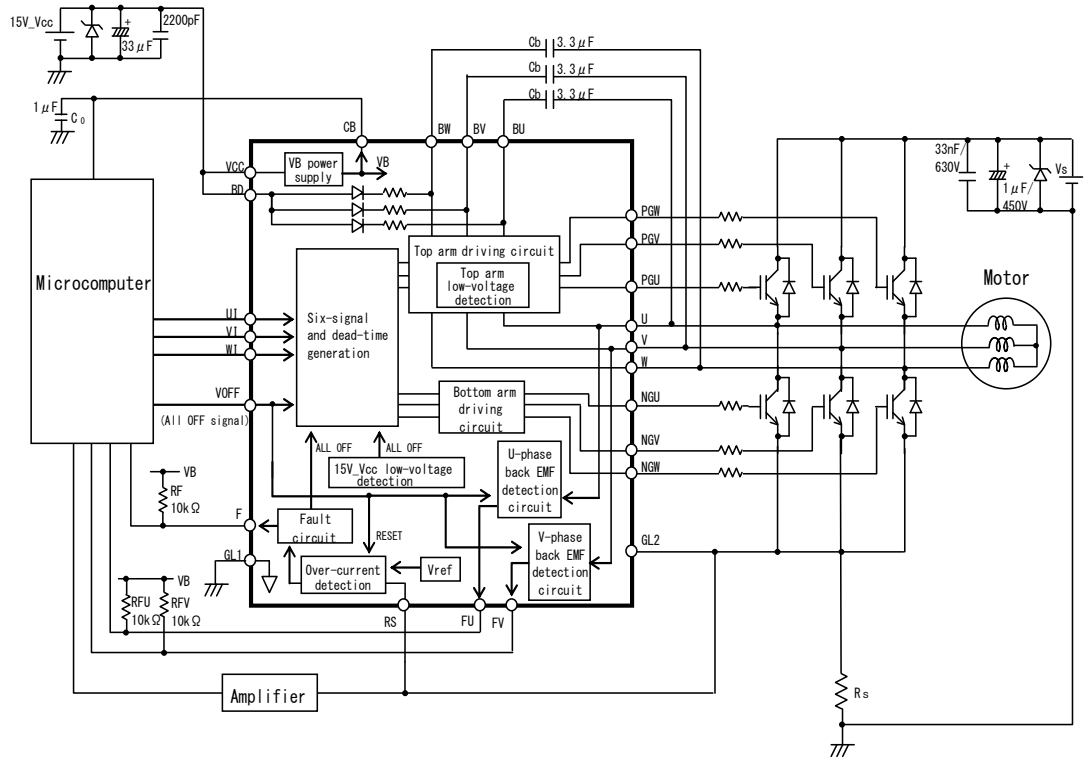


FIGURE 3.1.1 Example of Recommended Circuit of ECN33550 (ECN33550 is shown inside the bold line)

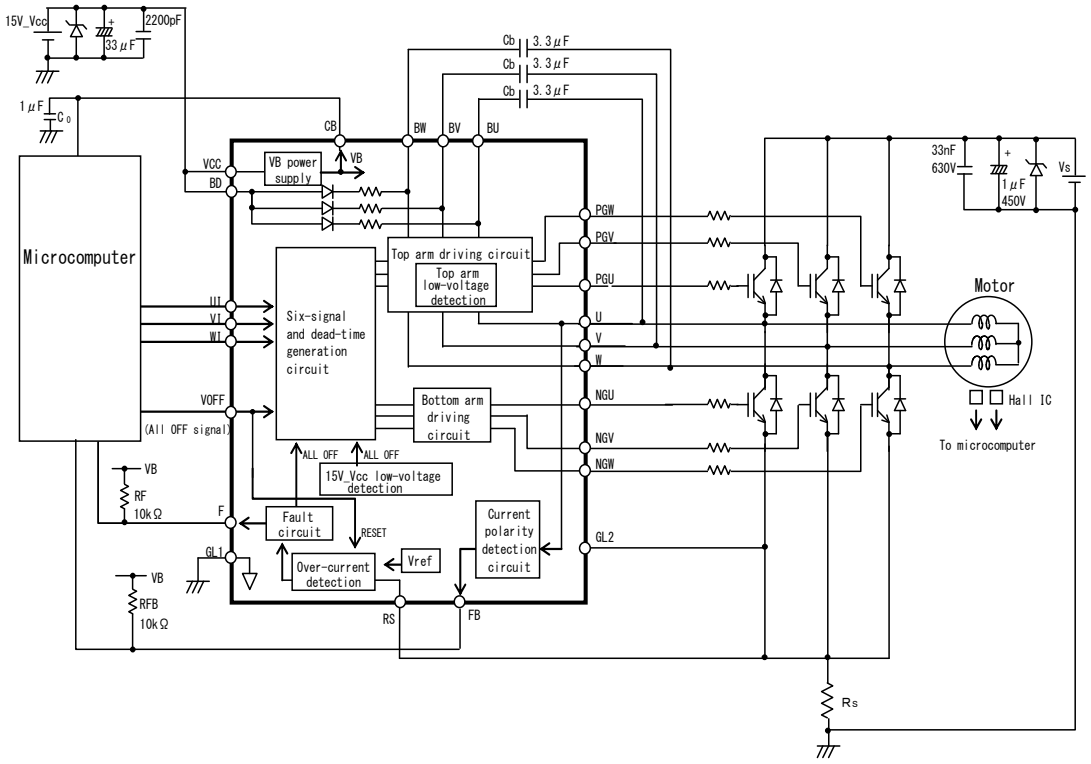


FIGURE 3.1.2 Example of Recommended Circuit of ECN33500 (ECN33500 is shown inside the bold line)

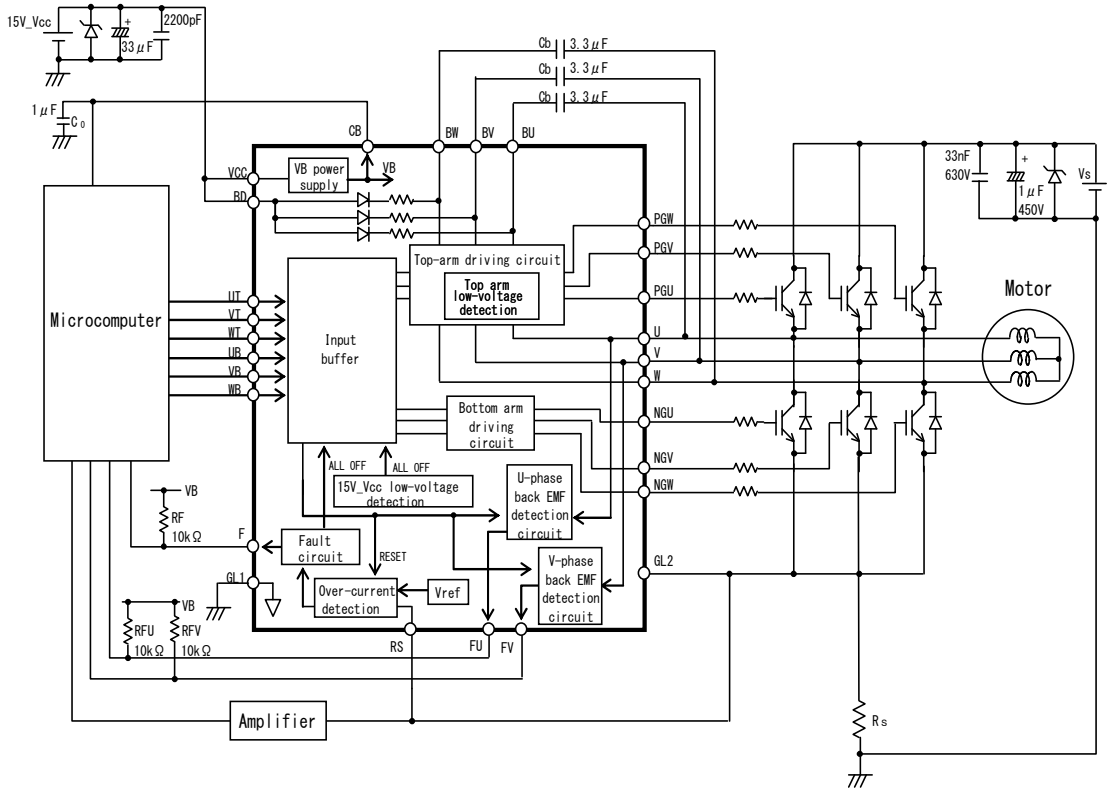


FIGURE 3.1.3 Example of Recommended Circuit of ECN30551 (ECN30551 is shown inside the bold line)

4. Failure Examples (Assumptions)

4.1 Gate Driver IC Destruction by an External Surge Inputted to Vs and 15V_Vcc Lines (Case 1)

・Cause : An external surge enters the gate driver IC on the Vs and 15V_Vcc lines of the motor. Because the Zener voltage of the surge suppressor diode is higher than the maximum rating voltage of the IC, it does not protect the IC.

・Phenomenon : The motor does not rotate due to the over-voltage destruction of the gate driver IC.

・Countermeasure : Use a surge suppressor diode with Zener voltage, which is lower than the maximum rating voltage of the gate driver IC. The larger the rating capacity of the Zener diode, the more effectively the surge suppressor works.

4.2 Gate Driver IC Destruction by an External Surge Inputted to Vs and 15V_Vcc Lines (Case 2)

・Cause : An external surge enters the gate driver IC on the Vs and 15V_Vcc lines of the motor. Because the capacity of the bypass capacitor for surge suppression is small, the surge cannot be sufficiently suppressed.

・Phenomenon : The motor does not rotate due to the over-voltage destruction of the gate driver IC.

・Countermeasure : Use the bypass capacitor for surge suppression; its capacity should be enough to suppress surges.

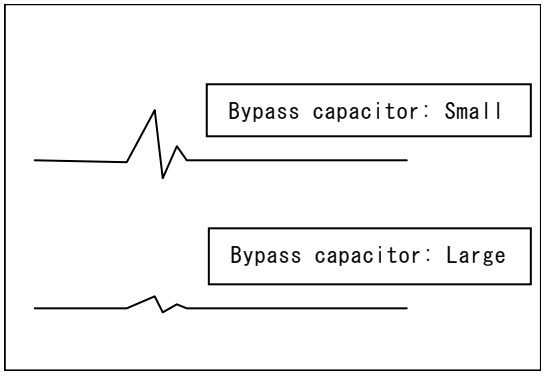


FIGURE 4.2.1 Example of Surge Waveforms for Different Bypass Capacitor Capacities

4.3 Gate Driver IC Destruction by an External Surge Inputted to Vs and 15V_Vcc Lines (Case 3)

・Cause : An external surge enters the gate driver IC on the Vs and 15V_Vcc lines of the motor. Because the external parts for surge suppression are positioned far from the gate driver IC on the board, the surge cannot be sufficiently suppressed.

・Phenomenon : The motor does not rotate due to the over-voltage destruction of the gate driver IC.

・Countermeasure: The bypass capacitor and Zener diode for surge suppression should be mounted close to the gate driver IC.

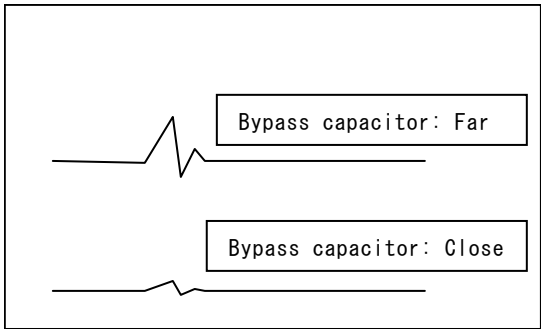


FIGURE 4.3.1 Example of Surge Waveform for Different Bypass Capacitor Locations on the Board

4.4 Gate Driver IC Destruction by 15V_Vcc Line Noise (Case 1)

・Cause : Pulsed noise of a voltage that is lower than the LVSD level enters the VCC line. In this case, the gate driver IC may repeat split-second LVSD operation. Then, the IC will have the possibility of causing the overheating destruction.

・Phenomenon : The motor does not rotate because the overheating destroys the output power device and gate driver IC.

・Countermeasure: ①Remove the noise that enters the motor 15V_Vcc line by reviewing the power supply circuit (inductance of power cable or the like).

②Connect a capacitor having sufficient capacity at a short distance between the VCC pin and GND pin of the gate driver IC to absorb noise.

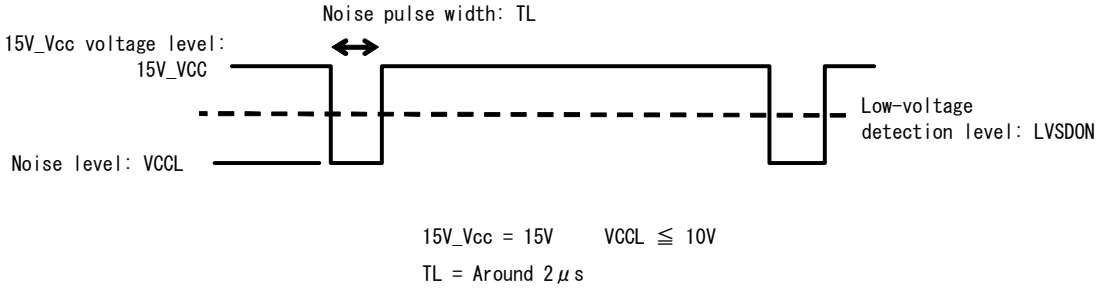


FIGURE 4.4.1 Example of Pulsed Noise on VCC at IC Destruction

4.5 Gate Driver IC Destruction by 15V_Vcc Line Noise (Case 2)

・Cause : Surge voltage that exceeds the maximum rating for the gate driver IC enters the VCC pin.

・Phenomenon : The motor does not rotate because the over-voltage destroys the gate driver IC.

・Countermeasure:

① Mount a bypass capacitor C1 near the pin of the gate driver IC. For more efficiency, use a capacitor that has good frequency characteristics, such as a ceramic capacitor. As a guide, a capacitor of around 1μF is recommended.

② It is more effective to mount a surge suppression device, such as bypass capacitor C2 shown in Fig. 4.5.1, close to the connector of a motor control circuit board to absorb a surge voltage of the 15V_Vcc.

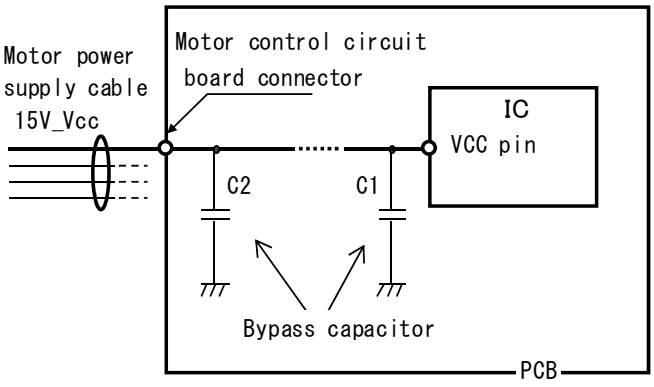


FIGURE 4.5.1 Example of Mounted Surge Suppression Devices

4.6 Gate Driver IC Destruction by Inspection Machine Relay Noise

・Cause : A mechanical relay for on-off control of the electric connection between the gate driver IC and an inspection machine generates a surge that enters the gate driver IC.

・Phenomenon : The motor does not rotate because the over-voltage destroys the gate driver IC.

・Countermeasure : Use a mercury relay, etc. Confirm a surge is not generated when the relay is on-off.

5. Precautions for Use

5.1 Countermeasures against Electrostatic Discharge (ESD)

(a) Customers need to take precautions to protect ICs from electrostatic discharge (ESD). The material of the container or any other device used to carry ICs should be free from ESD, which can be caused by vibration during transportation. Use of electrically conductive containers is recommended as an effective countermeasure.

(b) Everything that touches ICs, such as the work platform, machine, measuring equipment, and test equipment, should be grounded.

(c) Workers should be high-impedance grounded (100kΩ to 1MΩ) while working with ICs, to avoid damaging the ICs by ESD.

(d) Friction with other materials, such as high polymers, should be avoided.

(e) When carrying a PCB with a mounted IC, ensure that the electric potential is maintained at a constant level using the short-circuit terminals and that there is no vibration or friction.

(f) The humidity at an assembly line where ICs are mounted on circuit boards should be kept around 45 to 75 percent using humidifiers or such. If the humidity cannot be controlled effectively, using ionized air blowers (ionizers) is effective.

5.2 Storage Conditions

The following conditions are applied to ICs.

(1) Before opening the moisture prevention bag (aluminum laminate bag)

Temperature: 5℃ to 35℃
Humidity: 85%RH or lower
Period: less than 2 years

(2) After opening the moisture prevention bag (aluminum laminate bag)

Temperature: 5℃ to 30℃
Humidity: 70%RH or lower
Period: less than 1 week

(3) Temporal storage after opening the moisture prevention bag

When ICs are stored temporarily after opening the bag they should be returned into the bag with desiccant within 10 minutes. Then, the open side of the bag should be folded under twice, and closed with adhesive tape. And it should be kept in the following conditions.

Temperature: 5℃ to 35℃
Humidity: 85%RH or lower
Period: less than 1 month

※When the period of (1) to (3) is expected to expire, it is recommended to store the ICs in a drying furnace (30%RH or lower) at ordinary temperature.

(4) Baking process

When the period of (1) to (3) has expired, the ICs should be baked in accordance with the following conditions. (However, when the ICs are stored in a drying furnace (30%RH or lower) at ordinary temperature, there is no need to bake.)

Do not bake the tape and the reel of the taping package because they are not heat resistant.

Transfer the ICs to a heat resistant container prior to baking.

Temperature: 125±5℃
Period: 16 to 24 hours

5.3 Maximum Ratings

Regardless of changes in external conditions during use of IC (the product of Hitachi Power Semiconductor Device, hereinafter called “HPSD’s IC”), the “maximum ratings” should never be exceeded when designing electronic circuits that employ HPSD’s IC. If maximum ratings are exceeded, HPSD’s IC may be damaged or destroyed. In no event shall Hitachi Power Semiconductor Device (hereinafter called “HPSD”) be liable for any failure in HPSD’s IC or any secondary damage resulting from use at a value exceeding the maximum ratings.

5.4 Derating Design

Continuous high-load operation (high temperatures, high voltages, large currents) should be avoided and derating design should be applied, even within the ranges of the maximum ratings, to ensure reliability.

5.5 Safe Design

The HPSD's IC may fail due to accidents or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy and measures to prevent misuse, in order to avoid extensive damage in the event of a failure.

5.6 Application

If HPSD's IC is applied to the following uses where high reliability is required, obtain the document of permission from HPSD in advance.

・Automobile, Train, Vessel, etc.

Do not apply HPSD's IC to the following uses where extremely high reliability is required.

・Nuclear power control system, Aerospace instrument, Life-support-related medical equipment, etc.

6. Notes Regarding this Document

(1) All information included in this document such as product data, diagrams, charts, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, specifications of products, etc. are subject to change without prior notice. Before purchasing or using any of the HPSD products listed in this document, please confirm the latest product information with a HPSD sales office.

(2) HPSD shall not be held liable in any way for damages and infringement of patent rights, copyright or other intellectual property rights arising from or related to the use of the information, products, and circuits in this document.

(3) No license is granted by this document of any patents, copyright or other intellectual property rights of any third party or of HPSD.

(4) This document may not be reprinted, reproduced or duplicated, in any form, in whole or in part without the express written permission of HPSD.

(5) You shall not use the HPSD products (technologies) described in this document and any other products (technologies) manufactured or developed by using them (hereinafter called "END Products") or supply the HPSD products (technologies) and END Products for the purpose of disturbing international peace and safety, including (i) the design, development, production, stockpiling or any use of weapons of mass destruction such as nuclear, chemical or biological weapons or missiles, (ii) the other military activities, or (iii) any use supporting these activities. You shall not sell, export, dispose of, license, rent, transfer, disclose or otherwise provide the HPSD products (technologies) and END Products to any third party whether directly or indirectly with knowledge or reason to know that the third party or any other party will engage in the activities described above.

When exporting, re-export transshipping or otherwise transferring the HPSD products (technologies) and END Products, all necessary procedures are to be taken in accordance with Foreign Exchange and Foreign Trade Act (Foreign Exchange Act) of Japan, Export Administration Regulations (EAR) of US, and any other applicable export control laws and regulations promulgated and administered by the governments of the countries asserting jurisdictions over the parties or transaction.

(6) HPSD has taken reasonable care in compiling the information included in this document, but HPSD assumes no liability whatsoever for any damage incurred as a result of errors or omissions in the information included in this document.

(7) Please contact a HPSD sales office if you have any questions regarding the information in this document or any other inquiries.