

3-phase IGBT/MOS Gate Driver IC

ECN30552/ECN30502

Application Note

【Rev. 0】

Hitachi Power Semiconductor Device, Ltd.
Design Development Division

— Contents —

| | |
|--|----|
| 1. Outline | 4 |
| 1.1 3-Phase IGBT/MOS Gate Driver IC (ECN30552/30502) Outline | 4 |
| 1.2 System Configuration | 4 |
| 1.3 Block Diagram of IC | 5 |
| 2. Content of Specifications | 6 |
| 3. Specifications | 6 |
| 3.1 Pin Assignments | 6 |
| 3.2 Functions of Pins | 8 |
| 3.3 Markings | 11 |
| 3.4 Functions and Operational Precautions | 11 |
| 3.4.1 Protection Function | 11 |
| 3.4.2 Bootstrap Power Supply | 16 |
| 3.4.3 Dead Time | 18 |
| 3.4.4 Internal Filter Circuit | 18 |
| 3.4.5 Back EMF Detection (Type : ECN30552)..... | 19 |
| 3.4.6 Current Polarity Detection (Type : ECN30502)..... | 19 |
| 3.4.7 VCB Power Supply | 20 |
| 3.4.8 Level Shift Circuit | 20 |
| 3.5 Precautions for Use | 21 |
| 3.5.1 Output Wiring | 21 |
| 3.5.2 Notes Regarding Input Pins..... | 21 |
| 3.5.3 Initial Setting in Turning on Power | 22 |
| 3.5.4 Increase in Capacity of Output Power Device | 22 |
| 3.5.5 Notes Regarding VCC Pin..... | 22 |
| 3.5.6 Notes Regarding GL1 Pin, GL2 Pin..... | 22 |
| 3.6 Calculation of Power Consumption and Junction Temperature..... | 23 |
| 3.6.1 Power Consumption | 23 |
| 3.6.2 Calculation of Junction Temperature | 23 |
| 3.7 Mounting | 24 |
| 4. Recommended Circuit | 25 |
| 4.1 External Components..... | 25 |
| 4.2 Other External Components..... | 26 |
| 5. Failure Examples (Assumptions) | 27 |
| 5.1 Gate Driver IC Destruction by External Surge Inputted to Vs and Vcc Lines (Case 1) | 27 |
| 5.2 Gate Driver IC Destruction by External Surge Inputted to Vs and Vcc Lines (Case 2) | 27 |
| 5.3 Gate Driver IC Destruction by External Surge Inputted to Vs and Vcc Lines (Case 3) | 27 |
| 5.4 Gate Driver IC Destruction by External Surge Inputted to Vcc Line (Case 1) | 28 |
| 5.5 Gate Driver IC Destruction by External Surge Inputted to Vcc Line (Case 2) | 28 |

5.6 Gate Driver IC Destruction by Vcc Line Noise28

5.7 Gate Driver IC Destruction by Inspection Machine Relay Noise29

6. Precautions for Use30

6.1 Countermeasures against Electrostatic Discharge (ESD).....30

6.2 Storage Conditions30

6.3 Maximum Ratings30

6.4 Derating Design30

6.5 Safe Design30

6.6 Application.....31

7. Notes Regarding this Document.....31

1. Outline

1.1 3-Phase IGBT/MOS Gate Driver IC (ECN30552/30502) Outline

These gate driver ICs are monolithic ICs integrating various devices and circuits, needed for inverter control, on a single chip. They are the ICs for driving gates of a three-phase bridge inverter circuit using MOSFETs (Metal Oxide Semiconductor Field Effect Transistor), IGBTs (Insulated Gate Bipolar Transistor) or other devices. The gate driver ICs are particularly suited for variable speed control of three-phase induction motors or DC brushless motors rated operating voltage ranging from 200V AC to 240V AC.

The ECN30552 and ECN30502 are 6-input types. They have a back electromotive force (hereinafter called “back EMF”) detection or a current polarity detection to feed back the motor information to a microcontroller (hereinafter called “MCU”).

Table 1.1.1 shows the differences in ECN30552 and ECN30502.

TABLE 1.1.1 Difference in ECN30552, ECN30502

| Type | Back EMF detection | Current polarity detection |
|----------|--------------------|----------------------------|
| ECN30552 | Yes | No |
| ECN30502 | No | Yes |

Figure 1.1.1 shows Type and Package of IC.

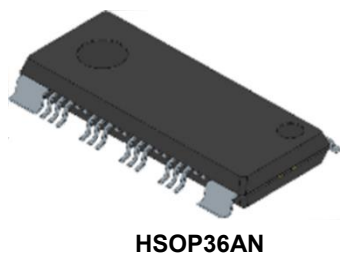


FIGURE 1.1.1 Type and Package of IC

1.2 System Configuration

An inverter is a device that converts DC currents into AC. It can be used to drive motors with efficient variable-speed control. Figure 1.2.1 shows the example of basic system configuration. The gate driver IC outputs the gate drive signals in accordance with the PWM signals from the MCU and drives an output power device consisting of six MOSFETs or IGBTs with the inverter.

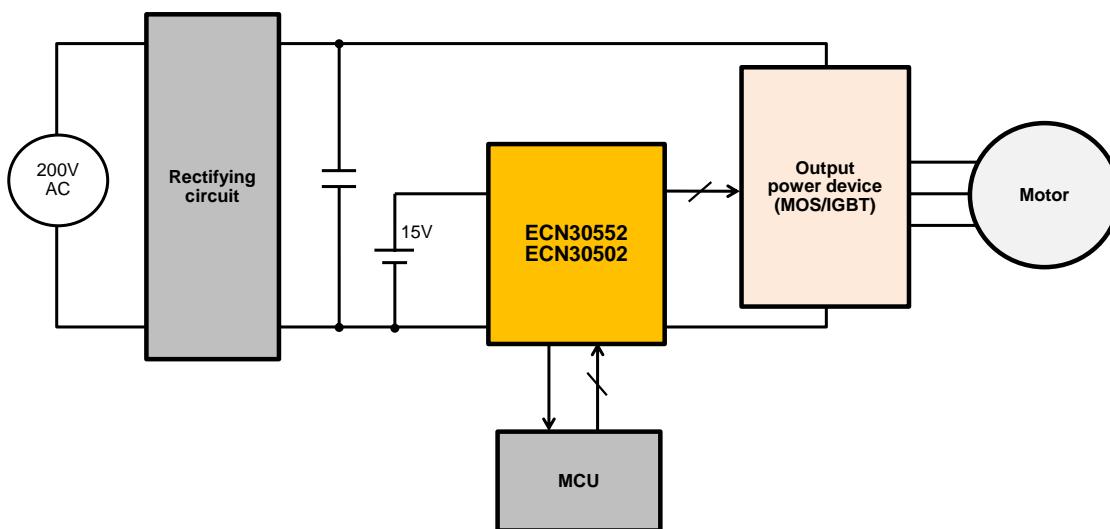


FIGURE 1.2.1 Example of Basic System Configuration

1.3 Block Diagram of IC

Figures 1.3.1 and 1.3.2 show block diagrams. The following devices and circuits are incorporated.

- Diodes for bootstrap
- Feedback circuit for motor information (Back EMF detection circuit: ECN30552)
(Current polarity detection circuit: ECN30502)

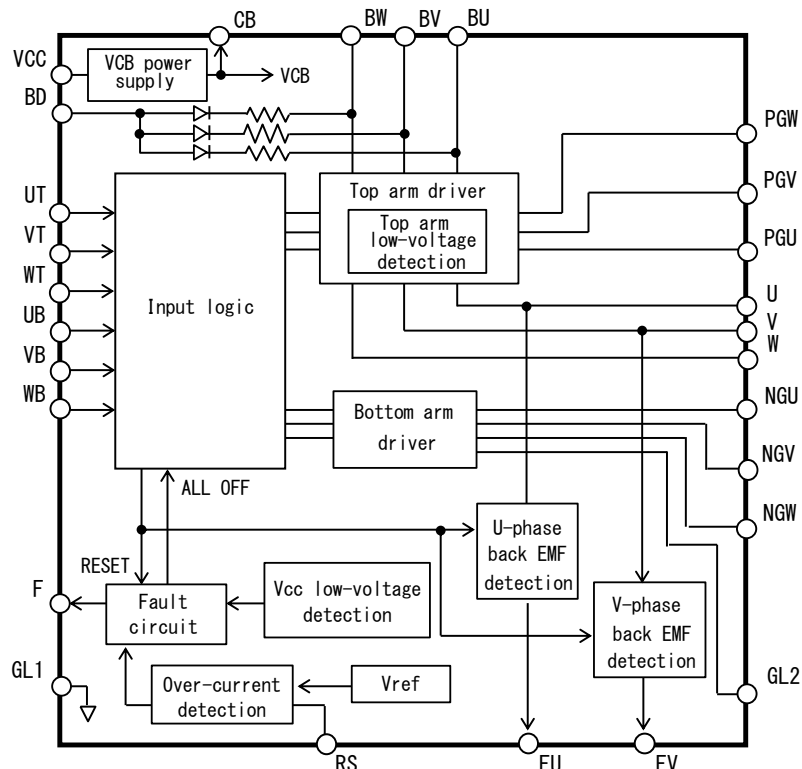


FIGURE 1.3.1 Block Diagram of IC (ECN30552)

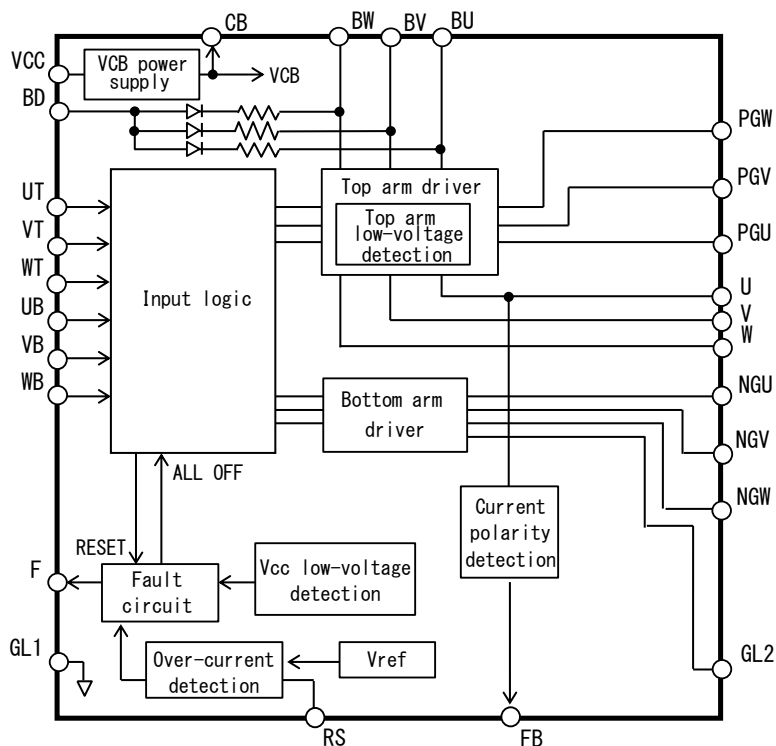


FIGURE 1.3.2 Block Diagram of IC (ECN30502)

2. Content of Specifications

The following items have been described in the specifications.

- (1) Maximum ratings
 - It describes direct conditions (electric, thermal use conditions) leading to IC destruction, and so on. And the safety operating range with operating conditions is shown by minimum or maximum value.
 - In a case the specified values shown in each item are exceeded, products may be damaged or destroyed even for a moment. These specified values should never be exceeded under any operating conditions.
- (2) Electrical characteristics
 - It provides for electric characteristics of the IC, and describes minimum, standard, and maximum.
- (3) Function and operation
 - It describes Truth Table, Timing Chart, Protection Function, and so on.
- (4) Standard application
 - It describes circuit examples and external components to operate IC.
- (5) Pin assignments and pin definitions
 - It describes pin assignments, pin names and pin definitions.
- (6) Inspection
 - It describes inspection conditions.
- (7) Important notice, precautions
 - It describes notes of the static electricity, the maximum rating, handling, and so on.
- (8) Appendix and reference data
 - It describes packaging and dimensions.

3. Specifications

3.1 Pin Assignments

Table 3.1.1 shows the pin assignments.

TABLE 3.1.1 Pin Assignments (1/2)

| Pin No. | Symbol | | Pin functions | Remarks |
|------------|--------|-------|--|------------|
| | 30552 | 30502 | | |
| 1,22,23,36 | GL1 | | Control system GND | |
| 2 | NC | | No connection | Note 2 |
| 3 | UT | | Input control signal for U-phase top arm | |
| 4 | VT | | Input control signal for V-phase top arm | |
| 5 | WT | | Input control signal for W-phase top arm | |
| 6 | UB | | Input control signal for U-phase bottom arm | |
| 7 | VB | | Input control signal for V-phase bottom arm | |
| 8 | WB | | Input control signal for W-phase bottom arm | |
| 9 | NC | | No connection | Note 2 |
| 10 | F | | Fault signal output | |
| 11 | FU | FB | FU: U-phase back EMF signal output / FB: Feedback signal (motor current polarity signal) output | FB: Note 3 |
| 12 | FV | NC | FV: V-phase back EMF signal output / NC: No connection | NC: Note 2 |

Note 1. High voltage pin

Note 2. Not connected to the chip in the IC.

Note 3: Used when controlling the motor using our software.

TABLE 3.1.1 Pin Assignments (2/2)

| Pin No. | Symbol | | Pin functions | Remarks |
|---------|--------|-------|---|---------|
| | 30552 | 30502 | | |
| 13 | RS | | Input for over-current protection | |
| 14 | CB | | VCB power supply output | |
| 15 | NC | | No connection | Note 2 |
| 16 | NC | | No connection | Note 2 |
| 17 | NC | | No connection | Note 2 |
| 18 | NC | | No connection | Note 2 |
| 19 | BD | | For bootstrap diode | |
| 20 | VCC | | Control power supply | |
| 21 | GL2 | | Reference pin of bottom arm outputs (connected to a current detection resistor) | |
| 24 | NGW | | W-phase bottom arm gate drive signal output | |
| 25 | NGV | | V-phase bottom arm gate drive signal output | |
| 26 | NGU | | U-phase bottom arm gate drive signal output | |
| 27 | W | | Reference pin of W-phase top arm output | Note 1 |
| 28 | BW | | W-phase top arm drive circuit power supply | Note 1 |
| 29 | PGW | | W-phase top arm gate drive signal output | Note 1 |
| 30 | V | | Reference pin of V-phase top arm output | Note 1 |
| 31 | BV | | V-phase top arm drive circuit power supply | Note 1 |
| 32 | PGV | | V-phase top arm gate drive signal output | Note 1 |
| 33 | U | | Reference pin of U-phase top arm output | Note 1 |
| 34 | BU | | U-phase top arm drive circuit power supply | Note 1 |
| 35 | PGU | | U-phase top arm gate drive signal output | Note 1 |

Note 1. High voltage pin.

Note 2. Not connected to the chip in the IC.

Note 3: Used when controlling the motor using our software.

3.2 Functions of Pins

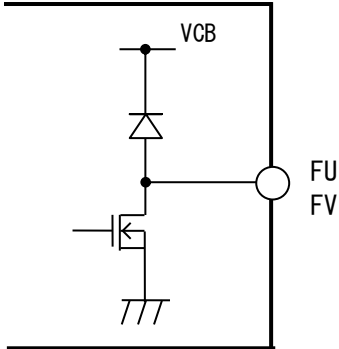
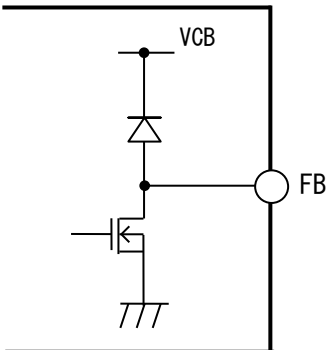
TABLE 3.2.1 List of Pins and Functions (1/3) [ECN30552/30502]

| No. | Pin | Items | Functions and Precautions | Related items | Remarks |
|-----|-------------------|---|---|---|------------------|
| 1 | VCC | Control power supply pin | <ul style="list-style-type: none"> • Powers the drive circuits for the bottom arms and the built-in VCB supply circuit, and others. • Determine the capacity of the power supply for Vcc allowing for a margin determined by adding the standby current Is1 and the current taken out of the CB pin. | <ul style="list-style-type: none"> • 3.4.1 (1) (a) Vcc low-voltage detection • 3.5.5 Notes regarding VCC pin • 5.1 to 5.5 Gate driver IC destruction by external surge or line noise | - |
| 2 | CB | VCB power supply output | <ul style="list-style-type: none"> • Outputs a voltage (typ. 5.0V) generated in the built-in VCB power supply. • VCB supply powers the IC internal circuits (input buffer, over-current protection and others) and can be used as a power supply for external circuits such as MCU, Hall elements, and so on. • Connect an oscillation prevention capacitor C0 (1.0μF \pm20% recommended) to the CB pin. | <ul style="list-style-type: none"> • 3.4.7 VCB power supply | - |
| 3 | GL1 | Control GND pin | <ul style="list-style-type: none"> • It is the ground pin for the Vcc and VCB power lines. | - | - |
| 4 | GL2 | Reference pin of bottom arm outputs | <ul style="list-style-type: none"> • Potential at this pin is reference potential of bottom arm outputs. • Connected to shunt resistor Rs, it monitors current and over current status. | <ul style="list-style-type: none"> • 3.4.1 (2) Over-current protection | - |
| 5 | RS | For over-current protection | <ul style="list-style-type: none"> • Detects over current status. When the voltage at the RS pin reaches the Vref (typ. 0.5V), the outputs of the top and bottom arms become all "L". | <ul style="list-style-type: none"> • 3.4.1 (2) Over-current protection | - |
| 6 | U V W | Reference pin of top arm output | <ul style="list-style-type: none"> • Reference potentials of each phase top arm output. • Connect these pins to outputs of each phase bridge circuit and motor coils. | - | High voltage pin |
| 7 | BU BV BW | Top arm drive circuit power supply pin | <ul style="list-style-type: none"> • Powers the drive circuits for the top arms. • Set the capacity of the bootstrap capacitor to an adequate value, allowing for charge current to the gate and switching conditions, etc. | <ul style="list-style-type: none"> • 3.4.1 (1) (b)Top arm low-voltage detection • 3.4.2 Bootstrap power supply | High voltage pin |
| 8 | BD | For bootstrap diode | <ul style="list-style-type: none"> • Connected to phase top arm drive circuit power supplies (BU, BV, BW) respectively through high voltage diodes and current limiting resistors. • Can be used for bootstrap by connecting to VCC pin. | <ul style="list-style-type: none"> • 3.4.2 Bootstrap power supply | - |
| 9 | PGU PGV PGW | Output pin for top arm gate drive signal | <ul style="list-style-type: none"> • Outputs gate drive signals for top arm output power devices of three-phase bridge circuit. • Outputs BU, BV, BW voltage based on the U, V, W pin potential in each phase. | <ul style="list-style-type: none"> • 3.5.1 Output wiring • 3.5.4 Increase in capacity of output power device | High voltage pin |
| 10 | NGU NGV NGW | Output pin for bottom arm gate drive signal | <ul style="list-style-type: none"> • Outputs gate drive signal for bottom arm output power devices of three-phase bridge circuit. • Outputs Vcc voltage based on the GL2 pin potential. | <ul style="list-style-type: none"> • 3.5.1 Output wiring • 3.5.4 Increase in capacity of output power device | - |

TABLE 3.2.1 List of Pins and Functions (2/3) [ECN30552/30502]

| No. | Pin | Items | Functions and Precautions | Related items | Remarks |
|-----|----------------------------------|---------------------------------------|---|--|---------|
| 12 | UT VT WT UB VB WB | Control signal input pin for each arm | <ul style="list-style-type: none"> Inputs control signals of each phase. The UT, VT, WT correspond to the top arm outputs. The UB, VB, WB correspond to bottom arm outputs. Input/output relation is "H" active. If the switching noise is monitored, mount a capacitor. The maximum rating of input voltage is $V_{CB}+0.5V$. | <ul style="list-style-type: none"> 3.5.2 Notes regarding input pins | - |
| | | | | | |
| 13 | F | Fault signal output | <ul style="list-style-type: none"> NMOS open drain output pin. Pull up to the CB pin or 5V through an external resistor R_F ($10k\Omega\pm 5\%$ recommended). Outputs "L" when the Vcc low-voltage detection or over-current protection operates. Outputs "H" in a normal state. | <ul style="list-style-type: none"> 3.4.1 (1) (a) Vcc low-voltage detection 3.4.1 (2) Over-current protection | - |
| | | | | | |

TABLE 3.2.1 List of Pins and Functions (3/3)

| No. | Pin | Items | Applicable type | Functions and Precautions | Related items | Remarks |
|-----|----------|--|-----------------|--|--|---------|
| 14 | FU FV | Output pin for back EMF signal | ECN30552 | <ul style="list-style-type: none"> • NMOS open drain output pin. Pull up to CB pin or 5V through an external resistor RFU, RFV (10kΩ±5% recommended). • Outputs U-phase and V-phase back EMF signal while the inverter stops the operation (UB, VB, WB, UT, VT, WT = L) • Outputs “H” when the U or V pin voltage is the VIH or more. Outputs “L” when the U or V pin voltage is the VIL or less. | <ul style="list-style-type: none"> • 3.4.5 Back EMF detection | - |
| | | | |  <p style="text-align: center;">FIGURE 3.2.3 Equivalent Circuit Around FU, FV Pins</p> | | |
| 15 | FB | Output pin for feedback signal (motor current polarity signal) | ECN30502 | <ul style="list-style-type: none"> • NMOS open drain output pin. Pull up to the CB pin or 5V through an external resistor RFB (10kΩ±5% recommended). • Outputs U-phase motor current polarity signal. • Outputs “L” when the motor current polarity is “negative”. Outputs “H” when the motor current polarity is “positive”. | <ul style="list-style-type: none"> • 3.4.6 Current Polarity Detection | - |
| | | | |  <p style="text-align: center;">FIGURE 3.2.4 Equivalent Circuit Around FB Pin</p> | | |

3.3 Markings

The resin surface of the IC is marked.

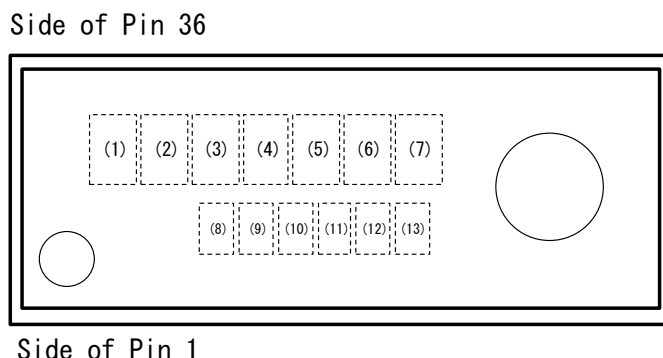


FIGURE 3.3.1 Marking Specifications

Mark No. (1) to (7) : Type name

Mark No. (8) to (13) : Lot number

The lot number consists of the followings.

No. (8)(9) : Last two digits of the year of assembly

No. (10) : Month of assembly:

January: A, February: B, March: C April: D, May: E, June: K,
July: L, August: M, September: N, October: X, November: Y, December: Z

No. (11) to (13) : Quality control number

Represented with letters from "A" to "Z" except "I" and "O", numbers from "0" to "9", or blank.

3.4 Functions and Operational Precautions

3.4.1 Protection Function

(1) Low-voltage detection

(a) Vcc low-voltage detection

Hitachi Power Semiconductor Device calls the Vcc low-voltage detection "LVSD". When the Vcc voltage drops below the LVSD operating voltage (LVSDON), the outputs of the top and bottom arms become all "L" and the F pin outputs "L". This function has hysteresis. This "All-L" state is reset when the Vcc voltage goes up to a level equal to or exceeding the LVSD recovery voltage (LVSDOFF) and the 6 input signals (UT, VT, WT, UB, VB, WB) are all held at "L" level for the Fault reset delay time (tflrs) or longer.

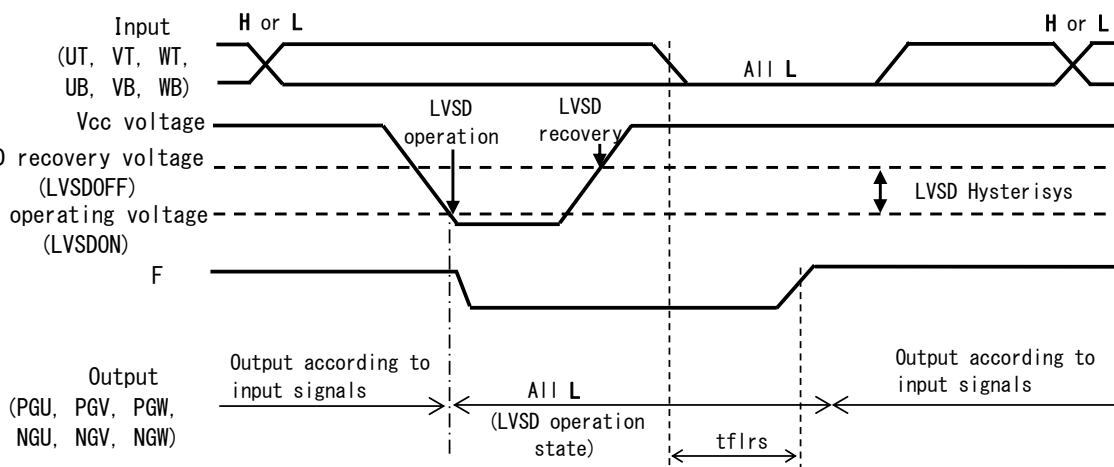


FIGURE 3.4.1.1 Timing Chart for Vcc Low-voltage Detection Operation (LVSD Operation)

(b) Top arm low-voltage detection

When the top arm power supply voltages (voltages between BU and U, BV and V, BW and W) drop below the operating voltage of the top arm low-voltage detection (LVSDONT), the top arm output of the corresponding phase becomes “L” even when the top arm input signals are “H”. This function has hysteresis. This “L” output state is reset when the “H” signal is inputted to the top arm after the top arm power supply voltages (voltages between BU and U, BV and V, BW and W) goes up above the recovery voltage of the top arm low-voltage detection (LVSDOFFT). However, even when the “L” output state is reset in a state in which the top arm input signal is “H”, the top arm is not turned on. This is because of latch function of top arm drive circuit (see Section 3.4.8 Level Shift Circuit). By inputting the “L” signal and then inputting the “H” signal again, the top arm is turned on. The Fault signal is not outputted in this function operation.

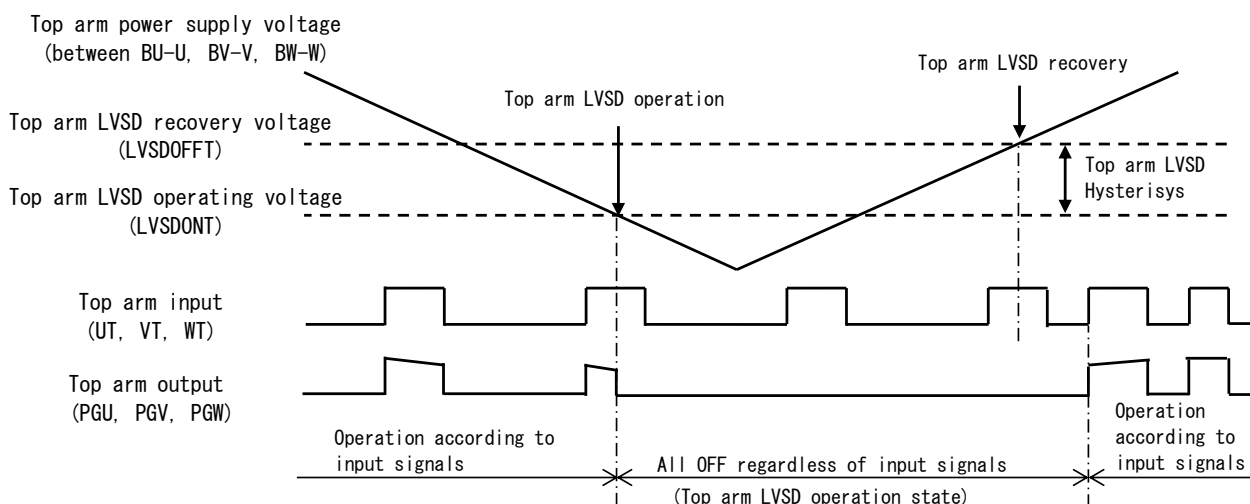


FIGURE 3.4.1.2 Timing Chart for Top Arm Low-voltage Detection Operation (Top arm LVSD Operation)

(c) Notice

If the Vcc low-voltage detection or the top arm low-voltage detection operates during motor rotation, Vs voltage may rise due to regenerative electric power to the Vs power supply. The Vs voltage must not exceed the maximum rating of the output power device. Particular attention is needed when the capacitance of a capacitor between the Vs and GND is small, because it makes the voltage more likely to rise.

(2) Over-current protection

(a) Over-current protection operation

This IC monitors the current through the shunt resistor R_s . When the voltage at the RS pin reaches the V_{ref} (Typ. 0.5V) of the internal detection circuit, the outputs of the top and bottom arms become all “L” and the F pin outputs “L”. This “All-L” state is reset when the 6 input signals (UT, VT, WT, UB, VB, WB) are all held at “L” level for the Fault reset delay time (t_{flrs}) or longer.

Just after the V_{cc} power supply is turned on, the over-current protection may operate. In this case, reset the “All-L” state in the same way as above.

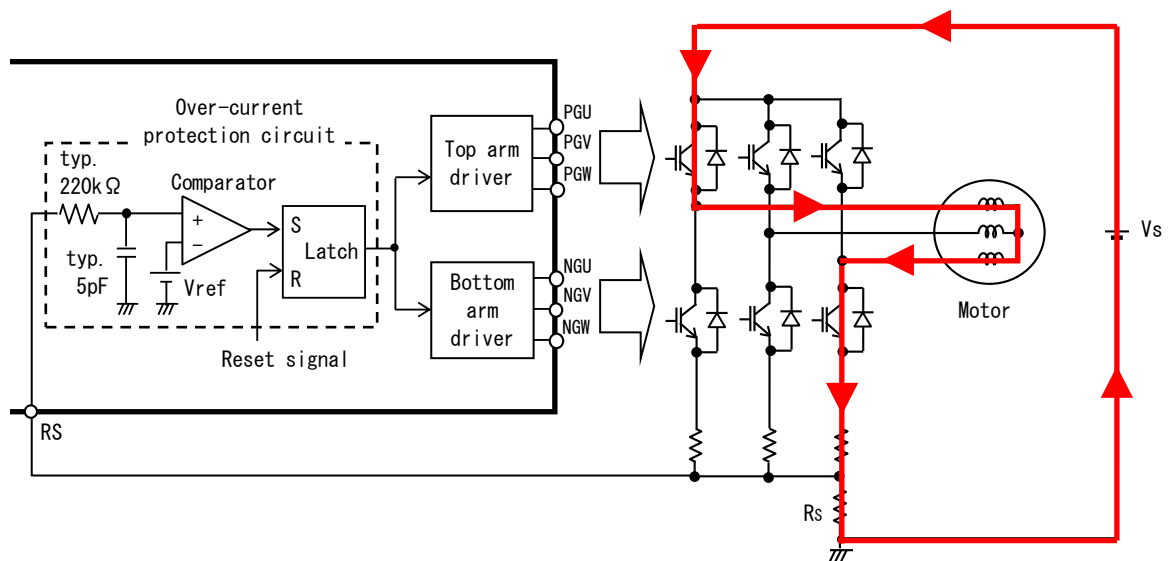


FIGURE 3.4.1.3 Example of Current Through Shunt Resistance

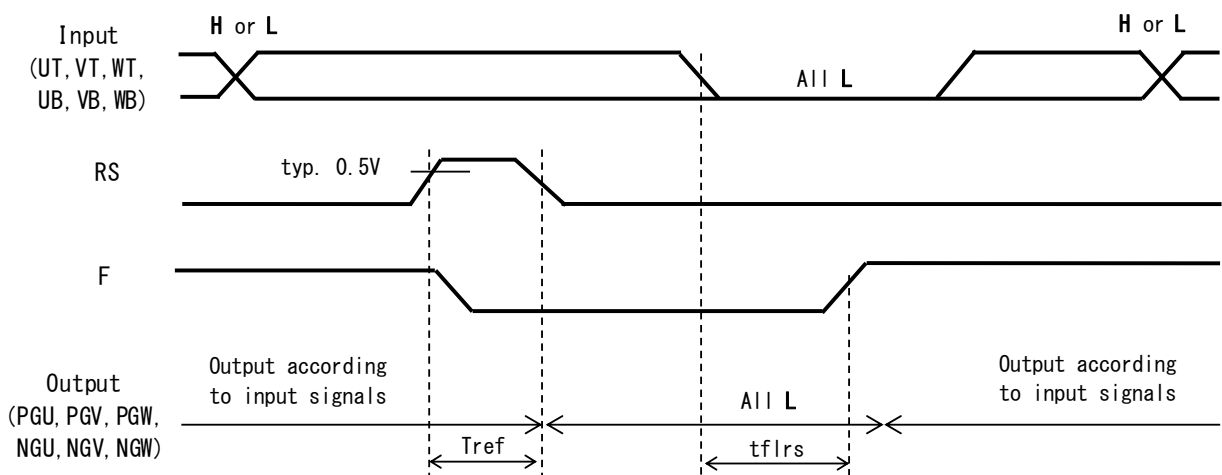


FIGURE 3.4.1.4 Timing Chart for Over-current Protection Operation

(b) How to set current value of over-current protection

The over-current protection set value (IO) is calculated as follows;

$$I_O = V_{ref}/R_s$$

V_{ref}: Over-current protection reference voltage

R_s : Shunt resistance value

In setting current values, delay time to turn the output power device off and variability of V_{ref} and R_s need to be considered. In practice, check the coil current of the motor. Set the shunt resistance so that voltage of the GL2 pin is within the specified voltage range of GL2 pin (V_{GL2}) in the product specification. This function is not effective for currents that do not flow forward (direction to the GL1 pin) through the shunt resistor, such as reflux current and power regenerative current (see Figures. 3.4.1.5 and 3.4.1.6).

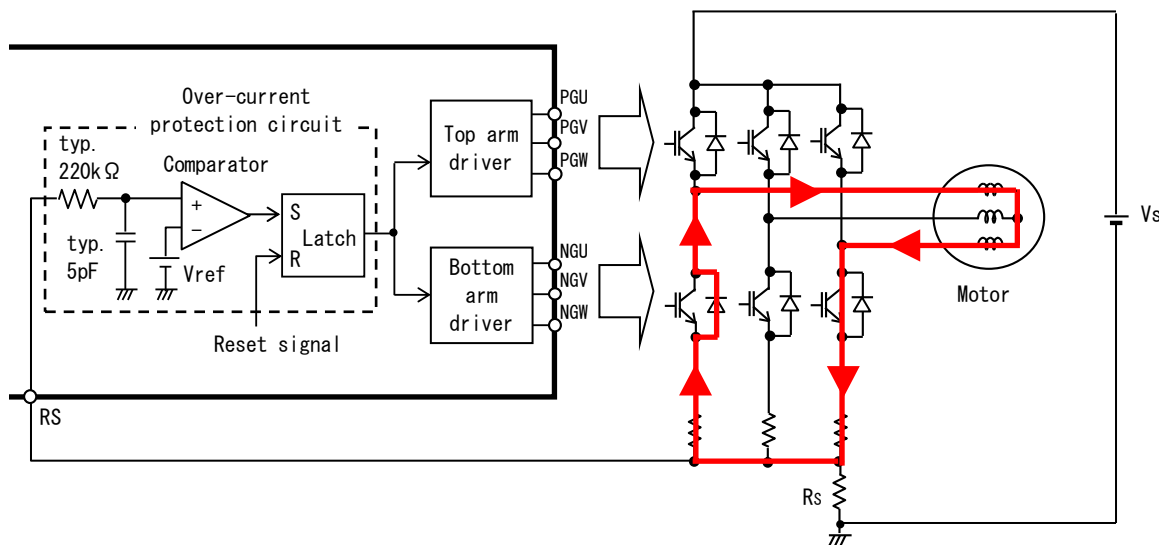


FIGURE 3.4.1.5 Example of Reflux Current

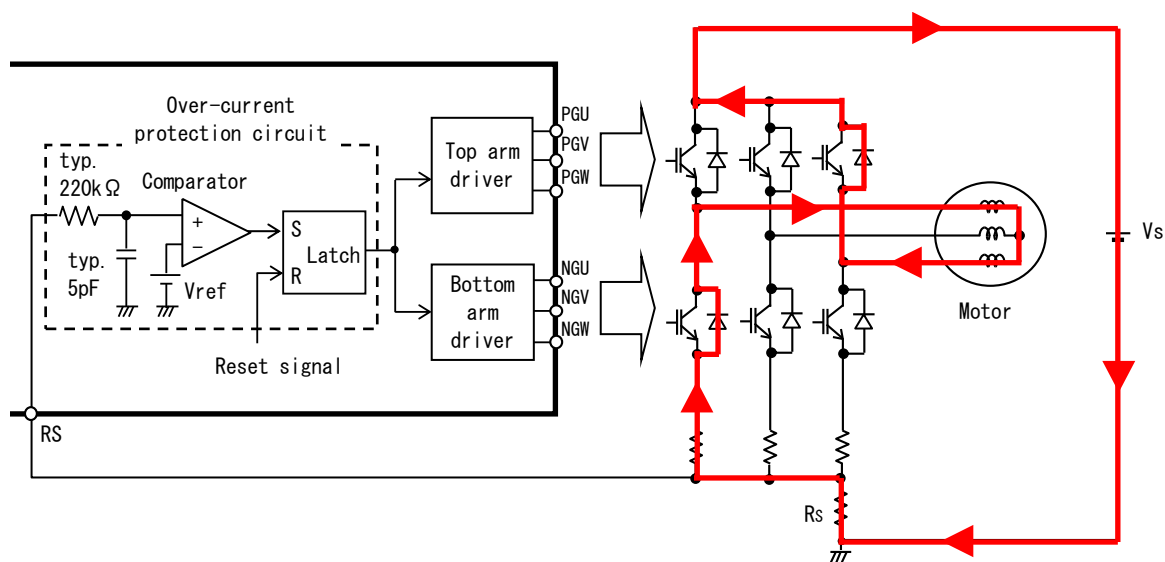


FIGURE 3.4.1.6 Example of Power Regenerative Current

(c) Precautions

• Shunt resistor R_s

Minimize the inductance of wiring of the shunt resistor R_s as far as possible (see Fig. 3.4.1.7). If the wiring has a high resistance or a high inductance, the emitter potential of the bottom arm IGBTs (source potential of MOS) changes, which can result in IGBT (MOS) malfunction.

When the over-current protection operates, minus surge voltage (V_a) may be generated in the shunt resistor R_s by this inductance (L_s) and the di/dt of current. This minus surge voltage (V_a) is applied between the GL1 pin and each of the GL2 pin, the bottom arm output pins NGU, NGV and NGW (through MOS/IGBT gate capacity coupling). This may destroy the IC in the worst case. This minus surge voltage (V_a) must not exceed $-5V$ between the GL1 pin and each of the GL2, NGU, NGV, and NGW pins. To suppress this minus surge voltage, effective measures are:

- ① to make the wiring of the shunt resistor R_s as short as possible,
- ② to use a non inductive shunt resistor, and
- ③ to clamp a surge voltage by adding the diode D_s in reversely parallel to the shunt resistor.

In this case, be aware that the effects depend on a connecting point and specification of a diode to be selected. It is recommended to use a fast recovery diode. Select its rating in according to a motor current.

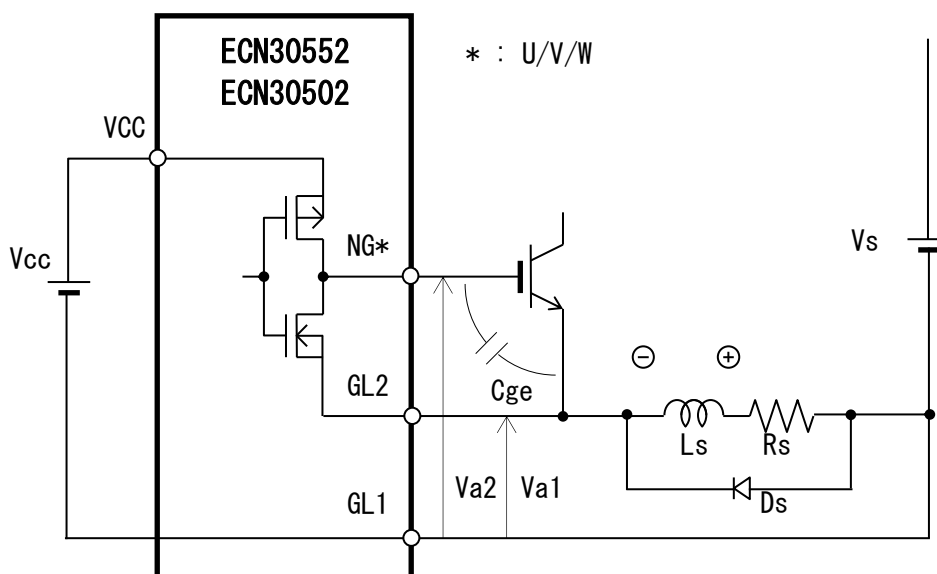


FIGURE 3.4.1.7 Over-voltage Generation Around Shunt Resistor

• Noise in R_s pin

The R_s pin is connected to a built-in CR filter having a time constant of about $1\mu s$. It is effective to add the CR filter externally if the over-current protection operates erroneously because of the effect of a noise and the like. However, note that adding the external CR filter increases the delay between the time the operating condition of the over-current protection is satisfied and the time the IGBTs are turned off.

3.4.2 Bootstrap Power Supply

(1) Outline of bootstrap power supply

A bootstrap system is a power supply method to the top arm drive circuit. By charging an external capacitor C_b , potential higher than the high power supply voltage (V_s) is obtained. Each negative side pin of the capacitors C_b is connected to a midpoint of each phase bridge circuit (the U, V, W pins), and each positive side pin is connected to the top arm power supply pin of each phase (BU, BV, BW) to charge the C_b using the control power supply V_{cc} .

Figure 3.4.2.1 shows the simplified circuit diagram of the bootstrap power supply for the top arm drive circuit. When the output power devices of the bottom arms are turned on, the capacitor C_b is charged (through passage ①). The output power device On-duty is limited because this charge in the capacitor C_b is consumed as a power supply for the top arm drive circuit. Bootstrap system is more superior in terms of cost compared to floating power supply as a power supply for the top arm drive circuit. However, it is necessary to charge the capacitor at an initial state in order to drive the top arm drive circuit.

The ON duration of the top arm output power device is affected by the capacitance of the capacitor C_b . Particular attention is needed when PWM carrier frequency is low.

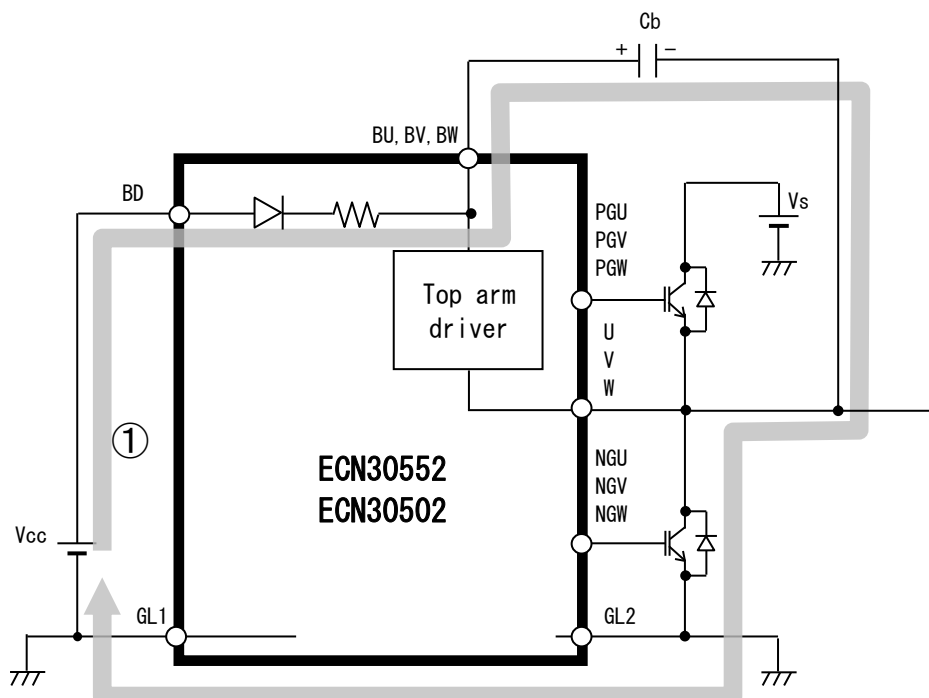


FIGURE 3.4.2.1 Bootstrap Power Supply

(2) Built-in bootstrap diode and current limiting resistor (BD pin)

As shown in Figures 1.3.1 and 1.3.2, the gate driver ICs incorporate high voltage diodes for bootstrap and current limiting resistors between the BD pin and each of the BU, BV, BW pins. Each resistance R_{bd} between the BD pin and each of the BU, BV, BW pins is about 75Ω . The voltage of the bootstrap capacitor C_b depends on the resistance R_{bd} , the On-duty of the output power device, and the capacitance of the capacitor C_b . Set the capacitance of the capacitor C_b and the On-duty in consideration of use conditions and use environment such that the bootstrap voltage does not go down to the maximum value of the top arm LVSD operating voltage (11.0V) or below while the inverter operates. (See the following subsection (3).)

It is also possible to mount the high voltage diode and the current limiting resistor as external components between the V_{cc} power supply and each of the BU, BV, BW pins without using the built-in bootstrap diodes or current limiting resistors. In this case, the BD pin must be held at a GND potential.

(3) Bootstrap circuit components

(a) Bootstrap capacitor Cb

Mount the Cb as close to the IC as possible to prevent the IC from being destroyed by over-voltage. An optimal capacity value of the bootstrap capacitor Cb varies depending on switching frequency, an On-duty of the output power device and a gate capacity. During the period from one charge to the next charge of the Cb, the top arm power supply voltage gradually goes down, because the charge accumulated in the capacitor Cb is consumed by a leakage current of the top arm drive circuit and the gate charge current of the top arm output power device. When the top arm power supply voltage goes down to the top arm low-voltage operating voltage, the top arm output is turned off. Therefore, the capacity value of the capacitor Cb is an important factor to prolong an ON-time of the top arms. The period from charging the Cb until the top arm is turned off is "tOnMax". This can be calculated using the following formula:

$$tOnMax = \{(VCb - LVSDONT) \times Cb - Q1 \times n\} / Is2$$

VCb : Top arm power supply voltage after charging

LVSDONT : Top arm low-voltage operating voltage

Cb : Capacitance of bootstrap capacitor

Q1 : Electric charge charged in output power device gate

n : The number of operation of top arm output power device

Is2 : Leakage current of the top arm drive circuit

Select the capacitance Cb of the bootstrap capacitor in accordance with the top arm maximum ON-time (tOnMax) and electric charge required for charging the output power device gates Q1. For reference, the calculated examples are shown below when VCb=15V, LVSDONT=11V, n=1 (once), Is2=30μA.

| Example of output power device | Gate charge Q1 (μC) | Cb (μF) | Top arm maximum ON-time tOnMax (ms) |
|--------------------------------|---------------------|---------|-------------------------------------|
| 600V/10A MOS | 0.040 | 1.0 | 132 |
| 600V/35A IGBT | 0.060 | 1.0 | 131 |
| 600V/35A IGBT | 0.060 | 3.3 | 438 |
| 600V/35A IGBT | 0.060 | 5.6 | 745 |

When adding a capacitor between the output pin of the IC and the output power device as shown in Fig. 3.5.1.1, consider a capacitance of the capacitor added.

When the number of operations of the top arm output power device is $n \geq 2$ (twice or more), the tOnMax becomes short because the larger the number of times of gate charging of the output power device is, the sooner the Cb is discharged. Under sine wave drive, the state will be generally "n=1" because the top and bottom arm output power devices operate alternately. However, when the PWM signal of the MCU and the operation of the output power device do not correspond, there is a possibility that " $n \geq 2$ " because either the top arm or bottom arm output power device operates. For example, in the narrow pulse width region of the PWM signal, this correspondence between the MCU PWM signal and the output power device operation is affected by the internal filter function of the gate driver IC (removing pulse having narrow pulse width in an input signal) and operation delays of the gate driver IC and the output power device. For this reason, it is estimated that the MCU PWM signal and the output power device operation do not correspond. When evaluating your system, a care (for example, check an On-duty and bootstrap voltage with actual output power device and select optimal capacitors Cb) is needed.

(b) Bootstrap current limiting resistor : Rb (When using external components of bootstrap diodes)

The Rb is important to limit the Cb initial charging current (inrush current) during the bootstrap operation. Make sure to insert the Rb because large inrush current adversely affects the system as described below.

① Destruction of bootstrap diode Db caused by surge current

Set the Rb to suppress the surge current below the allowable surge current value of the diode.

② Malfunction of over-current protection

The Cb inrush current flows through the bottom arm output power device to the shunt resistor for over-current detection. When this current exceeds the over-current detection level, the IC performs the over-current protection. Adjust the Rb to suppress the inrush current to be below the over-current detection level.

③ Destruction of top arm drive circuit caused by over-voltage

If the inrush current is large, over-voltage is generated during switching operations of the output power device under the influence of wiring reactance, which may result in gate driver IC destruction. Restrain the inrush current and take measures such as mounting the capacitor C_b close to the IC so as not to cause over-voltage.

(c) Bootstrap diode : D_b (When using external components)

Recommended diode D_b is: Withstand voltage = 600V or higher

Forward voltage = sufficiently small

Reverse recovery time t_{rr} = 100ns or less

If the forward voltage is large, the top arm power supply voltage drops. If t_{rr} is large, the D_b reverse recovery current I_{rr} flows into the V_{cc} power supply when the top arm output power device is turned on. This decreases efficiency of the bootstrap power supply. Determine your application by evaluating your system.

3.4.3 Dead Time

Each phase has two output power devices which have a totem pole configuration. If the top and bottom arm of the same phase are simultaneously turned on, short-circuit current flows. This may destroy the output power devices and a gate driver IC. Therefore, when the output control is shifted from top arm (bottom arm) OFF to bottom arm (top arm) ON in the same phase, it is necessary to secure the period the top and bottom arms in the same phase are OFF (dead time).

The gate driver IC incorporates a logic circuit capable of prohibiting the top and bottom arms from outputting the ON signals simultaneously. (A dead time is not generated.) This circuit works based on only the input signals, and does not work for delays of the gate driver IC output nor the output power device operation. Set a dead time in the input signals such that the top and bottom arm outputs of the output power devices are never ON simultaneously in any case.

3.4.4 Internal Filter Circuit

Internal filter circuits are located before the top and bottom arm drive circuits in these gate driver ICs. The filter circuits remove switching noise and narrow pulse signals inputted to the control signal input pins of each arm of the gate driver IC (UT, VT, WT, UB, VB, WB). As a guide, pulse width removed by the filter circuits is equal to or shorter than the turn-on/off output delay time of each phase.

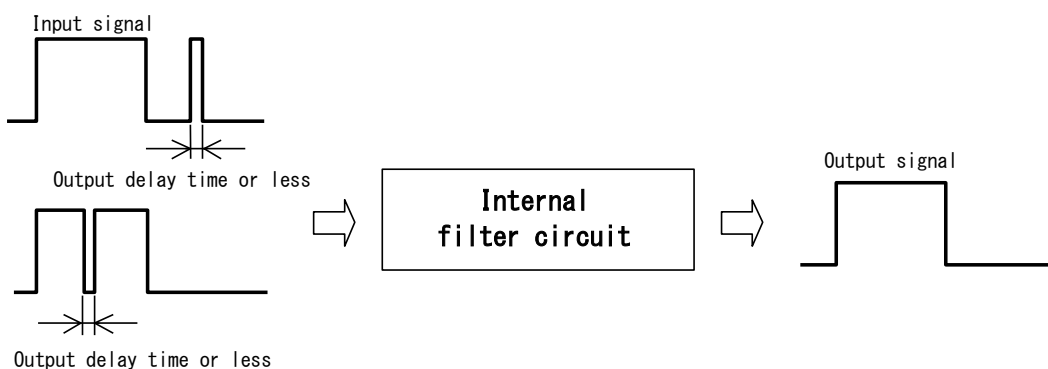


FIGURE 3.4.4.1 Internal Filter Circuit Operation

3.4.5 Back EMF Detection (Type : ECN30552)

When an external force makes the motor rotate (free-running) while the inverter stops operating, the back EMF signals are outputted as information on the rotor position. The U-phase back EMF signal and V-phase back EMF signal are outputted from the FU and FV pins respectively. Figure 3.4.5.1 shows a timing chart. The condition which the gate driver IC outputs the back EMF signals is satisfied when the inputs of the UB, VB, WB, UT, VT and WT pins are all "L". In the other conditions, you must not use the signals from the FU and FV pins as the information on the rotor position. When motor speed is decreased and the back EMF goes down below the detection level (VILE), the FU and FV pin outputs are "L". In using this signal, consider motor variance and detection level variance.

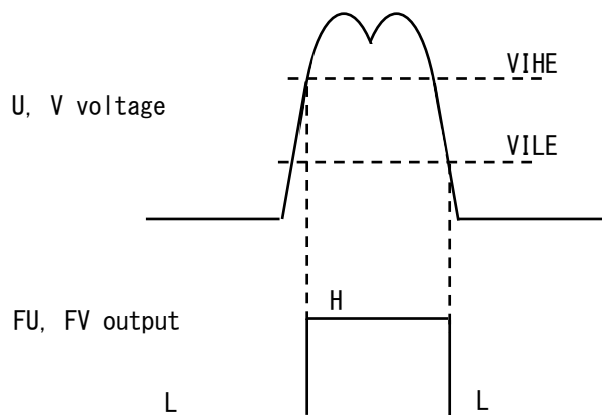


FIGURE 3.4.5.1 Timing Chart for Motor Output (U, V) and FU, FV Pin Signal Output

3.4.6 Current Polarity Detection (Type : ECN30502)

The FB pin outputs the U-phase current polarity signal as the phase information of the motor current while the inverter is operating. Regarding the motor current polarity, it is assumed that the direction from the output power device side to the motor coil side is set to positive, the direction from the motor coil side to the output power device side is set to negative. When the motor current polarity is "positive", the FB pin outputs "H". When the motor current polarity is "negative", the FB pin outputs "L".

The current polarity signal detects the U-phase current polarity based on the voltage at the U pin. The detection timing is immediately before* the rise of the U-phase top arm gate drive signal (PGU). *0.1μs to 0.5μs before

When a time after the gate driver IC outputs a gate drive signal until the output power device operates is too long, there is a possibility that current polarity signal information cannot be detected accurately.

When the current polarity is negative, adjust a gate resistor, gate capacity and dead time such that the output power device operation is completed 0.5μs or longer before the rise of the U-phase top arm gate drive signal (PGU). See Fig. 3.4.6.1.

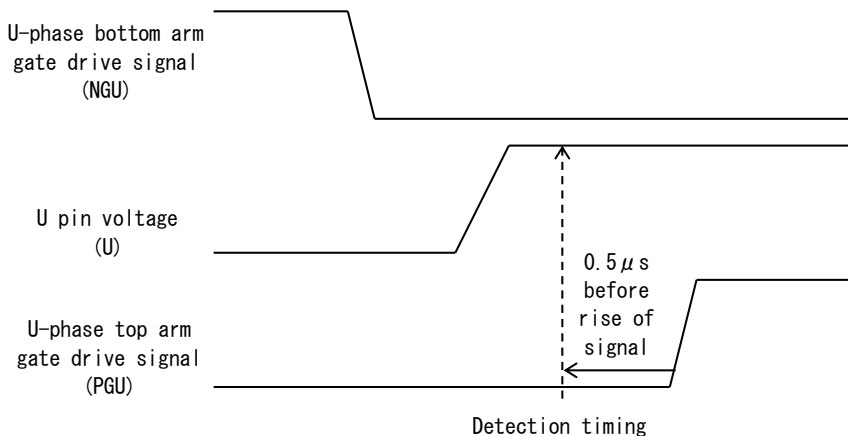


FIGURE 3.4.6.1 Detection Timing when Motor Current Polarity Signal "Negative"

3.4.7 VCB Power Supply

The VCB power supply is generated from Vcc power supply and outputted from the CB pin. The VCB power is supplied to the IC internal circuits such as the over-current protection circuit. Figure 3.4.7.1 shows an equivalent circuit. This circuit constitutes a feedback circuit.

To prevent oscillation, connect capacitor C0 to the CB pin. The recommended capacitance for the C0 is $1.0\mu\text{F}\pm 20\%$. The larger the C0 capacity, the more stable the VCB power supply. However, excessive capacitance is not recommended. As a guide, it should be $2\mu\text{F}$ to $3\mu\text{F}$ or less.

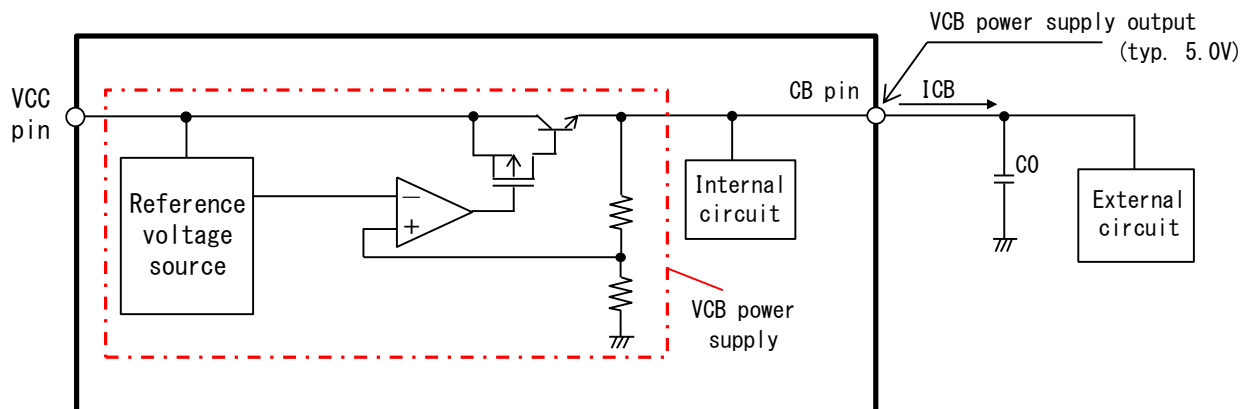


FIGURE 3.4.7.1 Equivalent Circuit for VCB Power Supply

3.4.8 Level Shift Circuit

Figure 3.4.8.1 shows the level shift circuit configuration. The level shift circuit converts the input signal based on GND level into the top arm gate drive signals based on the U, V, W voltage of each phase at floating potential. The drive circuit of the high voltage NMOS (a) and NMOS (b) for level shift uses a latch circuit that is triggered at rising edges of the input signals in order to reduce the current consumption of the level shift circuit.

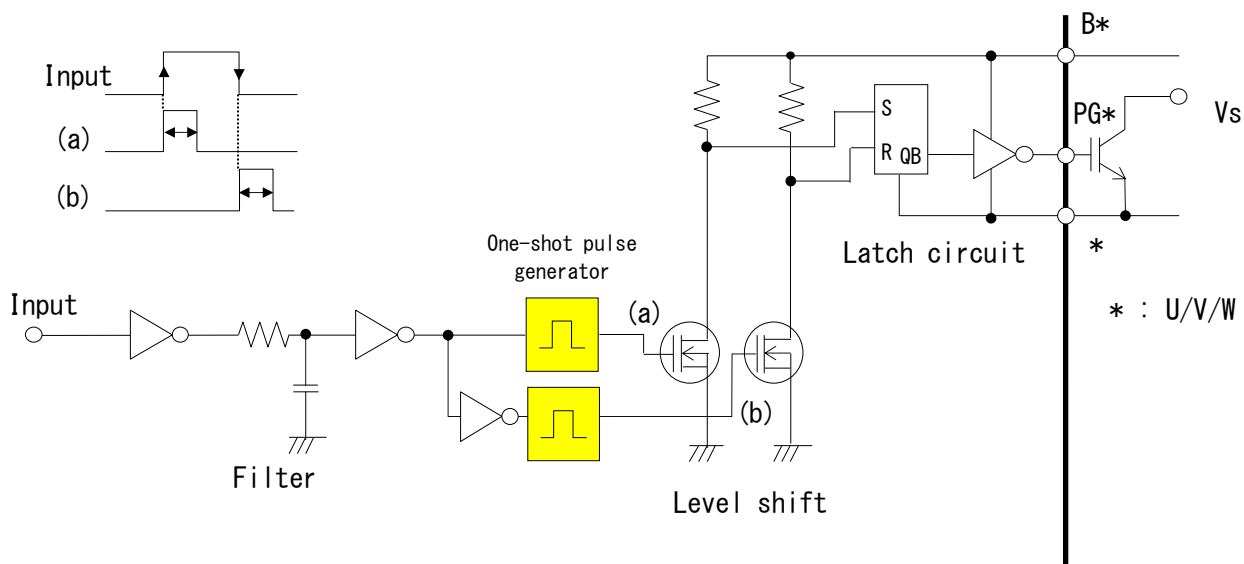


FIGURE 3.4.8.1 Configuration of Level Shift Circuit

3.5 Precautions for Use

3.5.1 Output Wiring

Make the wiring for connecting between the output pin of the gate driver IC and the output power device as short as possible in order to minimize the inductance. The output voltage of the gate driver IC may be oscillated at the frequency determined based on the wire inductance L_w and the gate capacity C_g of the output power device. This oscillating voltage could lead to destruction of the IC. If oscillations are observed, suppress the voltage oscillations such as by connecting the following components close to the top and bottom arm output pins of each phase of the IC as shown in Fig. 3.5.1.1.

- Capacitor CP (e.g., 560pF. Adjust the value in accordance with conditions of use.)
- Gate series resistor Rg (e.g., 100Ω. Adjust the value in accordance with conditions of use.)

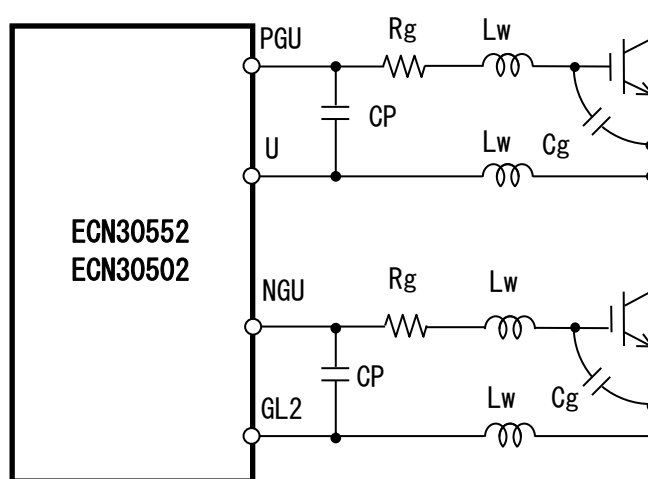


FIGURE 3.5.1.1 Addition of Capacitor CP for Preventing Oscillation and Resistor Rg (U-phase shown)

3.5.2 Notes Regarding Input Pins

The input pins (UT, VT, WT, UB, VB, WB) operate at a CMOS logic level of the internal regulator voltage VCB of the gate driver IC. If you use an external power supply for the MCU for control, be careful that the voltage of the input signal does not exceed the maximum rating of the input pin (-0.5V to VCB+0.5V) due to factors such as the fluctuations in the external power supply voltages.

These input pins are susceptible to the dv/dt noise in a switching operation of the output power device because they have large impedance. Therefore, when designing a printed circuit board (PCB), take anti-noise measures on a PCB such that switching noise of the output power device does not enter at the input pins. Any noise entering at the pins will cause improper operation, overheat, and over-voltage of the IC, which could result in the IC destruction.

It is effective to insert the filter (shown in Fig. 3.5.2.1) onto the input pins against switching noise. In this case, attention must be paid to risk of short circuits of the top and bottom arms, because the input pulses are delayed. Since a large current flows when a short circuit occurs, the ground line is oscillated, which could lead to over-voltage in the gate driver IC.

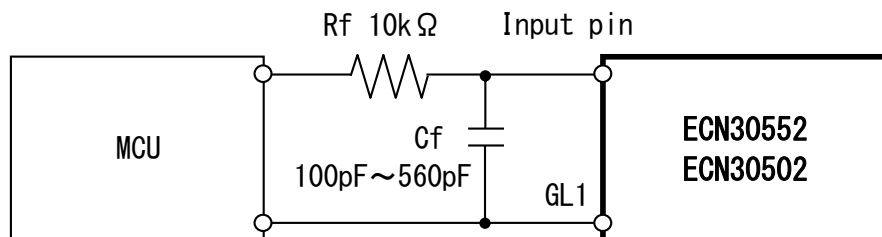


FIGURE 3.5.2.1 Example of Input Filter Insertion

3.5.3 Initial Setting in Turning on Power

When the Vcc power supply is turned on, set the following pins to be all OFF (UT, VT, WT, UB, VB, WB=L). After the Vcc power supply becomes stable, input the ON signal.

The top arm power supply voltage must be higher than the recovery voltage of the top arm low-voltage detection (LVSDOFFT). Therefore, it is necessary to initially charge the capacitor Cb before the inverter operation. The capacitor Cb is charged by turning on the bottom arm of the corresponding phase. The ON-time of bottom arm during initial charging is set based on the time constant calculated by multiplying Rbd by Cb ($Rbd \times Cb$). The Rbd represents the resistance between the BD pin and each of the BU, BV, BW pins (when using an external component, the Rbd depends on characteristics of an external component). As an initial setting after the power supply is turned on, it is recommended to input a bottom arm On-pulse width which is 3 times or more of $T=Rbd \times Cb$. Alternatively, inputting at least 3 bottom arm On-pulses of $T=Rbd \times Cb$ is also recommended.

3.5.4 Increase in Capacity of Output Power Device

In theory, the capacity of the output power device can be increased by connecting an external CMOS buffer to the output pin of the IC. However, when the capacity is increased, fast large current switching is likely to cause surge voltage and oscillation, and a possibility that could lead to malfunction or destruction of the gate driver IC becomes higher. Therefore, consider noise and over-voltage suppression before increasing the capacity of the output power device.

3.5.5 Notes Regarding VCC Pin

The VCC pin supplies output current, and whenever the output of the gate driver IC is turned on, the pulse current, whose peak is several hundred mA, flows. If there is wiring inductance in the VCC pin wiring, the noise of $L \times di/dt$ occurs at the VCC pin of the IC by the pulse current. When this noise exceeds the maximum rating of the Vcc, the IC may be destroyed. To avoid this, take measures to minimize the inductance. In addition, connect the capacitor as close to the VCC pin as possible. It is effective to mount a plurality of ceramic capacitors (bypass capacitor) of several hundred picofarads (pF) to several microfarads (μF) connected in parallel with an electrolytic capacitor. As a guide, the capacity of the electrolytic capacitor should be 10 times or more of the bootstrap capacitor Cb.

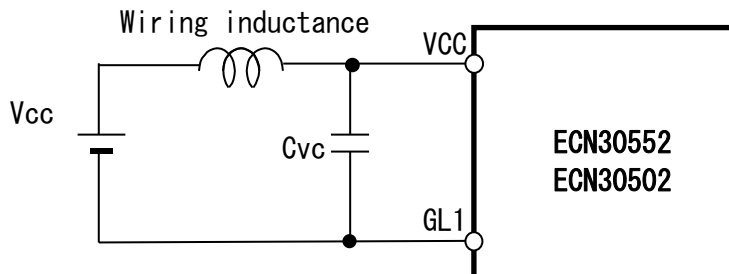


FIGURE 3.5.5.1 Addition of Capacitor for Vcc Power Supply

3.5.6 Notes Regarding GL1 Pin, GL2 Pin

The GL1 pin is control GND pin connected to Pin 1, Pin 22, Pin 23 and Pin 36 in the package. Connect a current detection resistor to the GL2 pin because the GL2 pin is a reference pin of bottom arm outputs. Wiring the GL1 pin wire and GL2 pin wire with a common solid pattern could result in malfunction. That is because of influence of voltage fluctuation at the GL2 pin through which large current flows. Separate the wirings of the GL1 pin and GL2 pin.

3.6 Calculation of Power Consumption and Junction Temperature

3.6.1 Power Consumption

A total power consumption of these ICs is classified roughly into following three items.

- (1) Power consumption caused by charging/discharging of gate capacity of external output power devices
- (2) Power consumption in high voltage circuits (level shifting circuits) in the IC
- (3) Power consumption in control circuit (Vcc voltage system circuit) in the IC

Figure 3.6.1.1 shows the calculation example of the power consumption under the following conditions.

Gate capacity of an output power device : C = 1000pF

Control power supply voltage : Vcc = 15V

High power supply voltage : Vs = 280V

PWM frequency : f_{PWM} = 1 kHz to 30 kHz

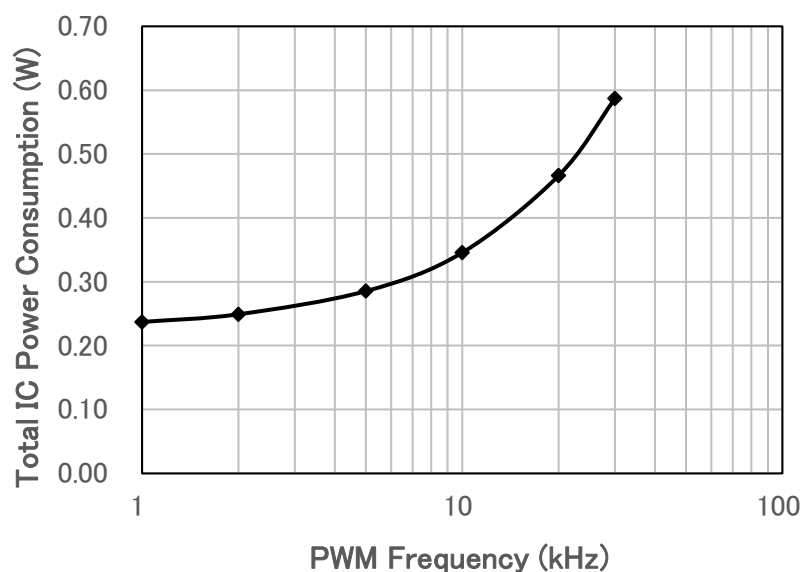


FIGURE 3.6.1.1 Calculation Example of Frequency-dependency of the Power Consumption

3.6.2 Calculation of Junction Temperature

A junction temperature can be calculated by the following equation after measuring the temperature of the IC case .

$$T_j = T_c + R_{jc} \times P$$

T_j : Junction temperature (°C)

T_c : IC case temperature (°C) (actual measurement)

R_{jc} : Thermal resistance of between junction and IC case (°C/W)

P : Total IC power consumption (W)

• Measuring method of T_c

A thermo-couple is set on the center of IC resin (top surface) to measure the IC case temperature T_c. After starting to apply a current, wait until the temperature becomes saturated (temperature stops rising). Use a value measured after temperature saturation.

3.7 Mounting

(1) Insulation between pins

High voltages are applied between the pin numbers specified below. Please apply coating resin or molding treatment as necessary.

Between pin numbers : 26-27, 29-30, 32-33, 35-36

(2) Tab suspension

Figure 3.7.1 shows a side view of the IC.

There are parts called "tab suspension" on both side surfaces of the IC. These tab suspensions are connected to the same potential as the GL pin. When the high voltage wire or/and components are laid out close to the tab suspensions, insulate them with coating, mold, or other treatment.

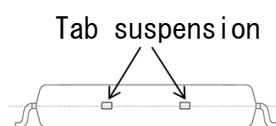


FIGURE 3.7.1 Side View of IC

(3) Coating resin

The influence of coating resin on semiconductor devices (thermal stress, mechanical stress and other stress) depends on PCB size, mounted components, etc. to be used. When selecting a coating resin, consult with your PCB manufacturer and resin manufacturer.

(4) Soldering conditions

The recommended reflow soldering condition is shown in Fig. 3.7.2.

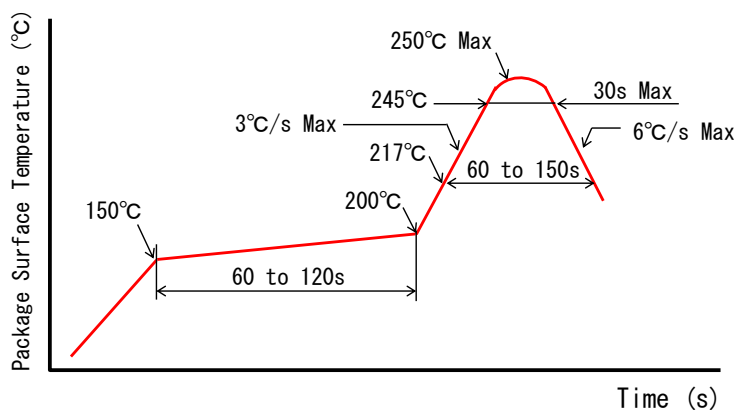


FIGURE 3.7.2 Recommended Conditions for Infrared Reflow or Air Reflow

(5) Solder joint reliability

Reliability of solder joints is influenced by soldering conditions, PCB material and foot patterns. Perform adequate evaluations on thermal cycle tests, heat shock tests, and other tests after mounting the IC on a PCB.

Special care should be taken if the HSOP36AN is mounted on a PCB having a high coefficient of thermal expansion (such as CEM-3) because the solder joint life could be shortened.

4. Recommended Circuit

4.1 External Components

Table 4.1.1 shows recommended external components.

TABLE 4.1.1 External Components

| Component | Standard value | Usage | Remarks |
|--------------|------------------|---|---------|
| Co | 1.0μF ± 20%, 25V | Smooths the internal power supply (VCB) | |
| Cb | 1.0μF ± 20%, 50V | For bootstrap | Note 1 |
| Rs | Note 2 | Sets over-current protection | |
| RF, RFU, RFV | 10kΩ ± 5% | For pull up | |

Note 1: The capacitance value of the bootstrap capacitor depends on the operating conditions.

Set the capacitance value taking into account the DC bias characteristics.

Note 2: The over-current protection set value (IO) can be calculated as follows.

$$IO = Vref / Rs \text{ (A)}$$

Figures 4.1.1 and 4.1.2 show block diagrams and external components. These are only indicative. Select peripheral components suitable for your system specifications and conditions of use, considering redundancy in design.

Adjust the settings of components in accordance with the conditions of use. Moreover, mount each of the components close to the pins of the IC to achieve the effect of the voltage surge absorption. Make the wiring between the shunt resistor Rs and the RS pin and between the RS pin and the GL2 pins as short as possible.

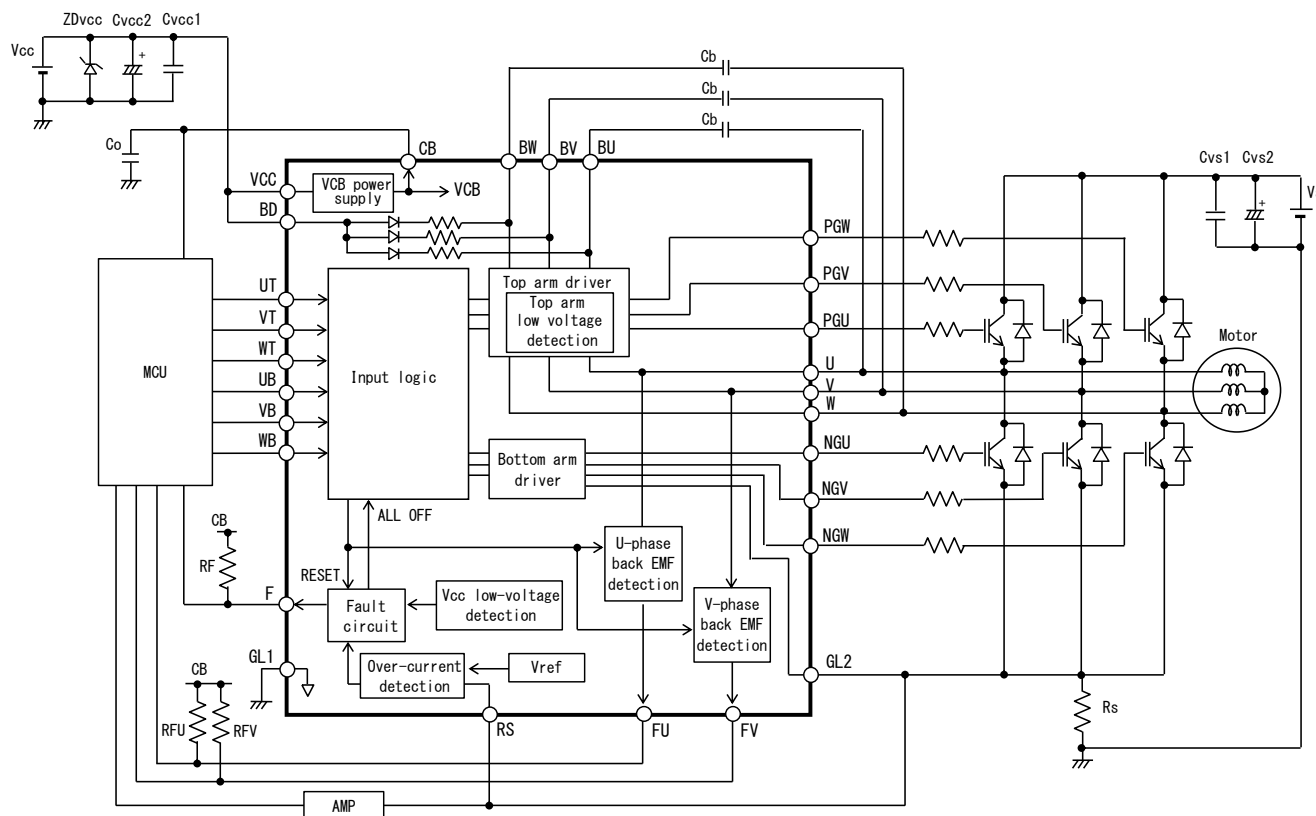


FIGURE 4.1.1 Block Diagram and External Components of IC (ECN30552)

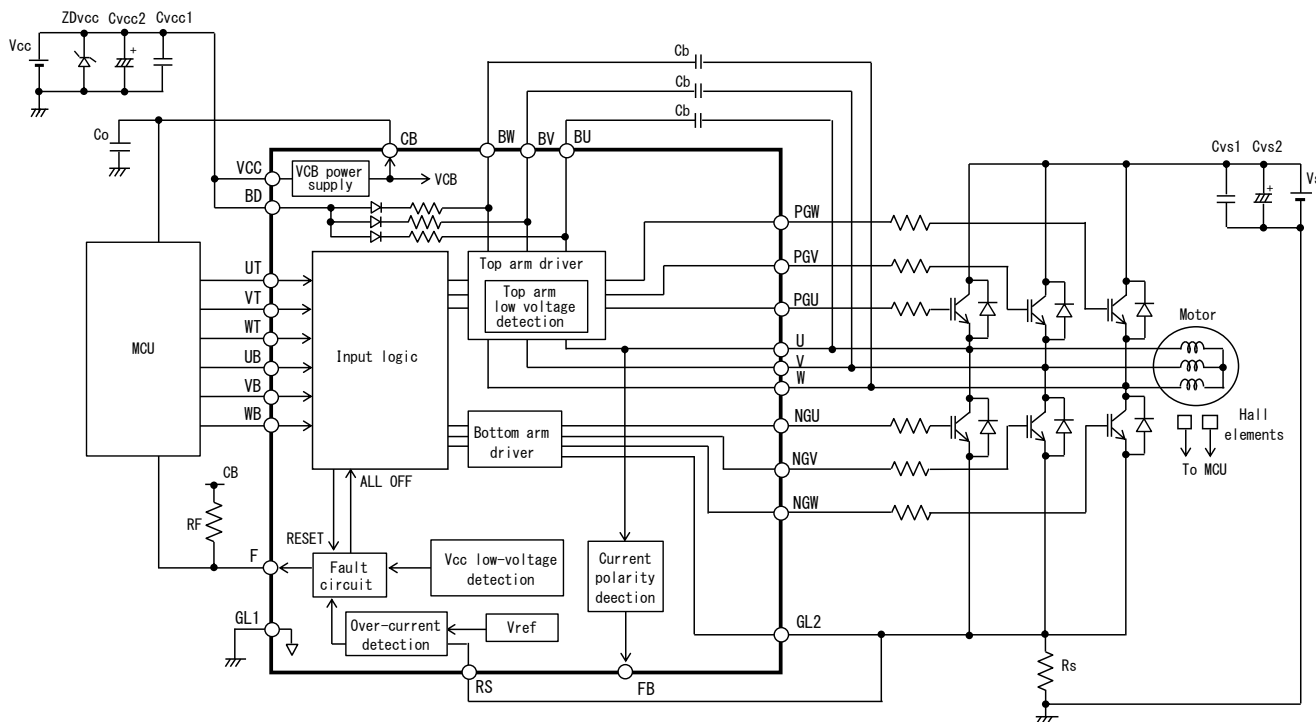


FIGURE 4.1.2 Block Diagram and External Components of IC (ECN30502)

4.2 Other External Components

It is recommended to mount the components shown in Table 4.2.1 to stabilize the power supply and protect the IC from voltage surge.

Adjust the settings of components in accordance with the conditions of use. Moreover, mount each of the components close to the pins of the IC to achieve the effect of the voltage surge absorption.

TABLE 4.2.1 Other External Components

| No. | Components | Purpose | Remarks |
|-----|------------|---|--|
| 1 | Cvcc1 | for VCC. To suppress high frequency noise | Ceramic capacitor with good frequency response, etc. About 2200pF |
| 2 | Cvcc2 | for VCC. To smooth Vcc power supply | Electrolytic capacitor, etc. About 33μF |
| 3 | ZDvcc | for VCC. To suppress over voltage | Zener diode with good frequency response |
| 4 | Cvs1 | for Vs. To suppress high frequency noise | Ceramic capacitor with good frequency response, etc. About 33nF/630V |
| 5 | Cvs2 | for Vs. To smooth Vs power supply | Electrolytic capacitor, etc. About 1μF/630V |

5. Failure Examples (Assumptions)

5.1 Gate Driver IC Destruction by External Surge Inputted to Vs and Vcc Lines (Case 1)

- Cause : An external surge entered the gate driver IC on the Vs and Vcc lines of the motor. Because the capacitance of the bypass capacitor for surge suppression was small, the surge could not be sufficiently suppressed.
- Phenomenon : The motor does not rotate due to the over-voltage destruction of the IC.
- Countermeasure : Use the bypass capacitor for surge suppression; its capacity should be enough to suppress surges.

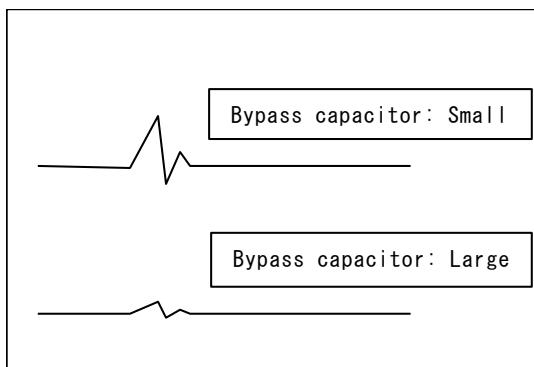


FIGURE 5.1.1 Example of Surge Waveforms for Different Capacitance of Bypass Capacitor

5.2 Gate Driver IC Destruction by External Surge Inputted to Vs and Vcc Lines (Case 2)

- Cause : An external surge entered the gate driver IC on the Vs and Vcc lines of the motor. Because the external parts for surge suppression were positioned far from the IC on the circuit board, the surge could not be sufficiently suppressed.
- Phenomenon : The motor does not rotate due to the over-voltage destruction of the IC.
- Countermeasure : The bypass capacitor and Zener diode for surge suppression should be mounted close to the IC.

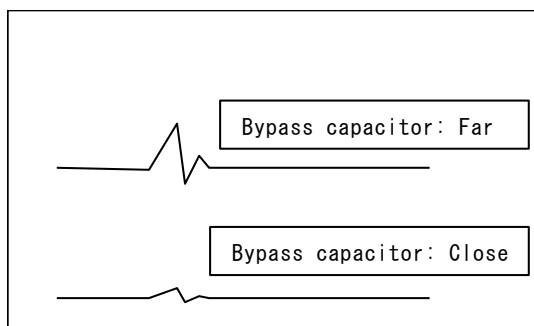


FIGURE 5.2.1 Example of Surge Waveform for Different Bypass Capacitor Locations on Board

5.3 Gate Driver IC Destruction by External Surge Inputted to Vs and Vcc Lines (Case 3)

- Cause : An external surge entered the gate driver IC on the Vs and Vcc lines of the motor. Because the Zener voltage of the surge suppressor diode was higher than the maximum rating voltage of the IC, it did not protect the IC.
- Phenomenon : The motor does not rotate due to the over-voltage destruction of the IC.
- Countermeasure: Use a surge suppressor diode with Zener voltage, which is lower than the maximum rating voltage of the IC. The larger the rating capacity of the Zener diode, the more effectively the surge suppressor works.

5.4 Gate Driver IC Destruction by External Surge Inputted to Vcc Line (Case 1)

- Cause : When a power supply line was in an open state due to the connector contact failure of Vcc line or the like, the supply power was turned on. Then, when the power supply line went into a closed state, a surge occurred and entered the gate driver IC.
- Phenomenon : The motor does not rotate due to the over-voltage destruction of the IC.
- Countermeasure: The Zener diode for surge suppression should be mounted close to the IC.

5.5 Gate Driver IC Destruction by External Surge Inputted to Vcc Line (Case 2)

- Cause : Pulsed noise of a voltage that was lower than the operating voltage of the Vcc low-voltage detection (LVSDON) entered the Vcc line. In this case, the IC repeats split-second LVSD operation. Then, the IC has the possibility of overhear breakage of the external inverter circuit and gate driver IC.
- Phenomenon : The motor does not rotate because the overheating destroys the external inverter and gate driver IC.
- Countermeasure: ① Remove the noise that enters the motor Vcc line by reviewing the power supply circuit (inductance of power cable or the like).
② Connect a capacitor having sufficient capacitance close to the VCC pin and GL1 pin of the IC to absorb noise.

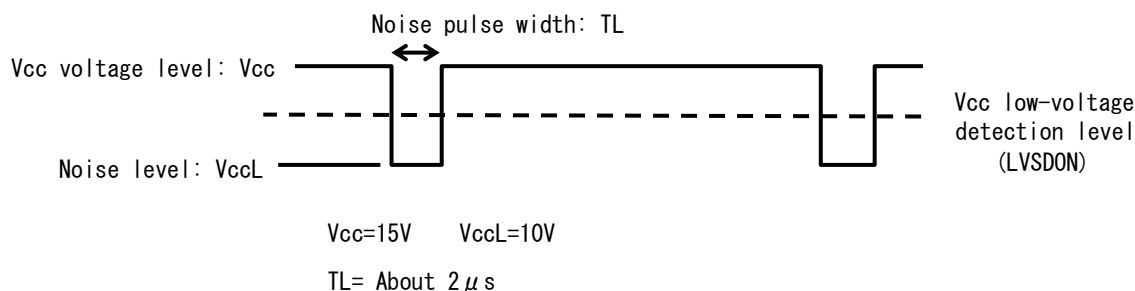


FIGURE 5.5.1 Example of Pulsed Noise on Vcc Line

5.6 Gate Driver IC Destruction by Vcc Line Noise

- Cause : Surge voltage that exceeded the maximum rating for the gate driver IC entered the VCC pin.
- Phenomenon : The motor does not rotate due to the over-voltage destruction of the IC.
- Countermeasure:
 - ① Mount a bypass capacitor C1 near the pin of the gate driver IC. Use a capacitor that has excellent frequency characteristics, such as a ceramic capacitor. As a guide, a capacitor of around 1 μ F is recommended.
 - ② It is more effective to mount a surge suppression device, such as bypass capacitor C2 shown in Fig. 5.5.1, close to the connector of a motor control circuit board.

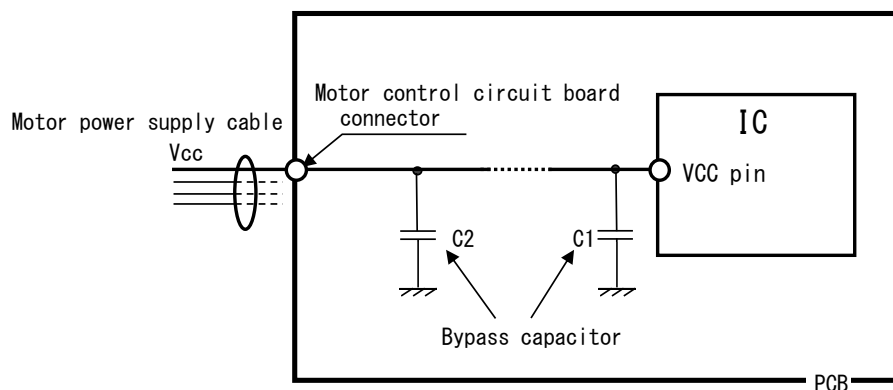


FIGURE 5.6.1 Example of Mounted Surge Suppression Devices

5.7 Gate Driver IC Destruction by Inspection Machine Relay Noise

- Cause : A mechanical relay for on-off control of the electric connection between the gate driver IC and an inspection machine generated a surge that entered the gate driver IC.
- Phenomenon : The motor does not rotate due to the over-voltage destruction of the IC.
- Countermeasure : Use a semiconductor relay, etc. Confirm a surge generated when the relay is on-off is less than the maximum rated value.

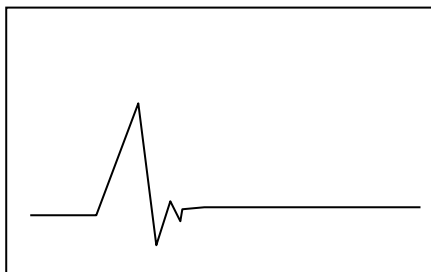


FIGURE 5.7.1 Example of Surge Waveform When Mechanical Relay is Used

6. Precautions for Use

6.1 Countermeasures against Electrostatic Discharge (ESD)

- (a) Customers need to take precautions to protect ICs from electrostatic discharge (ESD). The material of the container or any other device used to carry ICs should be free from ESD, which can be caused by vibration during transportation. Use of electrically conductive containers is recommended as an effective countermeasure.
- (b) Everything that touches ICs, such as the work platform, machine, measuring equipment, and test equipment, should be grounded.
- (c) Workers should be high-impedance grounded (100kΩ to 1MΩ) while working with ICs, to avoid damaging the ICs by ESD.
- (d) Friction with other materials, such as high polymers, should be avoided.
- (e) When carrying a PCB with a mounted IC, ensure that the electric potential is maintained at a constant level using the short-circuit terminals and that there is no vibration or friction.
- (f) The humidity at an assembly line where ICs are mounted on circuit boards should be kept around 45 to 75 percent using humidifiers or such. If the humidity cannot be controlled effectively, using ionized air blowers (ionizers) is effective.

6.2 Storage Conditions

- (1) Before opening the moisture prevention bag (aluminum laminate bag)

Temperature: less than 40 °C
 Humidity: less than 90%RH
 Period: less than 12 months

- (2) After opening the moisture prevention bag (aluminum laminate bag)

Temperature: 5 °C to 30 °C
 Humidity: less than 60%RH
 Period: less than 168 hours

※ When the period of (1) and (2) is likely to expire, store ICs in a drying furnace (10%RH or lower) at ordinary temperature.

- (3) Baking process

When the period of (1) and (2) has expired, ICs should be baked in accordance with the following conditions. (However, when ICs are stored in a drying furnace (10%RH or lower) at ordinary temperature, there is no need to bake.)

Do not bake the tape and the reel of the taping package because they are not heat resistant.

Transfer ICs to a heat resistant container prior to baking.

Temperature: 125 °C to 135 °C
 Period: more than 48 hours

6.3 Maximum Ratings

Regardless of changes in external conditions during use of IC (the product of Hitachi Power Semiconductor Device, hereinafter called "HPSD's IC"), the "maximum ratings" should never be exceeded when designing electronic circuits that employ HPSD's IC. If maximum ratings are exceeded, HPSD's IC may be damaged or destroyed. In no event shall Hitachi Power Semiconductor Device (hereinafter called "HPSD") be liable for any failure in HPSD's IC or any secondary damage resulting from use at a value exceeding the maximum ratings

6.4 Derating Design

Continuous high-load operation (high temperatures, high voltages, large currents) should be avoided and derating design should be applied, even within the ranges of the maximum ratings, to ensure reliability.

6.5 Safe Design

The HPSD's IC may fail due to accidents or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy and measures to prevent misuse, in order to avoid extensive damage in the event of a failure.

6.6 Application

If HPSD's IC is applied to the following uses where high reliability is required, obtain the document of permission from HPSD in advance.

- Automobile, Train, Vessel, etc.

Do not apply HPSD's IC to the following uses where extremely high reliability is required.

- Nuclear power control system, Aerospace instrument, Life-support-related medical equipment, etc.

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