HITACHI
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High Voltage 3-Phase Gate Driver IC
Application Guide
Rev. 0

Applicable models

For ≅ AC230V	**ECN30531F** **ECN30541F**

Hitachi Power Semiconductor Device, Ltd.

Precautions for Safe Use and Notices

If semiconductor devices are handled inappropriate manner, failures may result. For this reason, be sure to read this "Application Guide" before use.

⚠ This mark indicates an item about which caution is required.

⚠ CAUTION This mark indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury and damage to property.

⚠ CAUTION

(1) Regardless of changes in external conditions during use "absolute maximum ratings" should never be exceed in designing electronic circuits that employ semiconductors. In the case of pulse use, furthermore,"safe operating area(SOA)"precautions should be observed.

(2) Semiconductor devices may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure.

(3) In cases where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment), safety should be ensured by using semiconductor devices that feature assured safety or by means of user's fail-safe precautions or other arrangement. Or consult Hitachi's sales department staff.

(If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst)

NOTICES

1. This Application Guide contains the specifications, characteristics(in figures and tables), dimensions and handling notes concerning power semiconductor products (hereinafter called "products") to aid in the selection of suitable products.
2. The specifications and dimensions, etc. stated in this Application Guide are subject to change without prior notice to improve products characteristics. Before ordering, purchasers are advised to contact Hitachi's sales department for the latest version of this Application Guide and specifications.
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Revision History

Rev.	Date	Page	Item No.	Revision
0	13-Dec-2011	—	—	Newly issued

Contents

1. Introduction

ECN30531F/30541F series is a high-voltage driver IC that can drive 3-phase MOS-gated devices to which converted AC200～230V power supplies are applied. The use of six external IGBTs or MOSFETs allows 3-phase induction motors and DC brushless motors to be controlled at variable speed. Figure 1.1 shows a basic block diagram of a typical ECN30531F/30541F system.

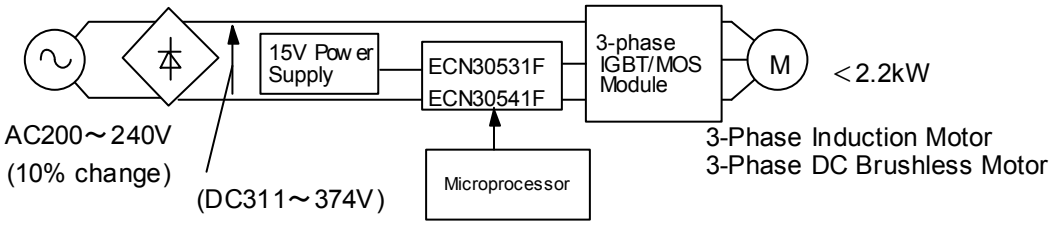

Figure 1.1 Configuration of a variable-speed control system with 3-phase motors

ECN30531F/30541F series can drive up to 30A IGBTs or MOSFETs, and control the speed of 3-phase motors with an output of up to 2.2kW at variable speed. The applicable motor output of a 3-phase induction motor can generally be determined by the following equation,

Motor output = $\sqrt{3} \times V_S \times I_M \times \cos\phi \times \eta$

V_S : DC voltage, I_M : Motor current, $\cos\phi$: Power factor≈0.8,

η : Motor efficiency≈0.8

2. ECN30531F/30541F series line-up

ECN30531F/30541F series offers a line-up of 2 types as listed in Table 2.1. Three types differ only in additional functions. Except for them, three types have the same main functions.

Table 2.1 ECN30531F/30541F series

Type	OP-Amp
ECN30531F	None
ECN30541F	Included

3. Driving by a floating power supply and by a bootstrap system

Each phase has two external IGBTs which have a totem pole configuration. In order to turn on IGBTs, the gate voltage needs to be higher than the threshold voltage Vth(about 5V) against the source voltage. The source of bottom arm IGBTs is fixed to the ground voltage. Therefore, they can be driven by applying Vcc voltage to the gate. However, in order to drive top arm IGBTs, the gate voltage needs to be higher than the Vs voltage because the source voltage of top arm IGBTs rises near to Vs. For this operation, the driving by a floating power supply and the driving by a bootstrap system can be applied. ECN30531F/30541F series can handle both types of driving.

3.1 Driving by a floating power supply

Three floating power supplies of VFU, VFV, VFW are needed. Figure 3.1.1 shows an example of a driving circuit for ECN30531F.

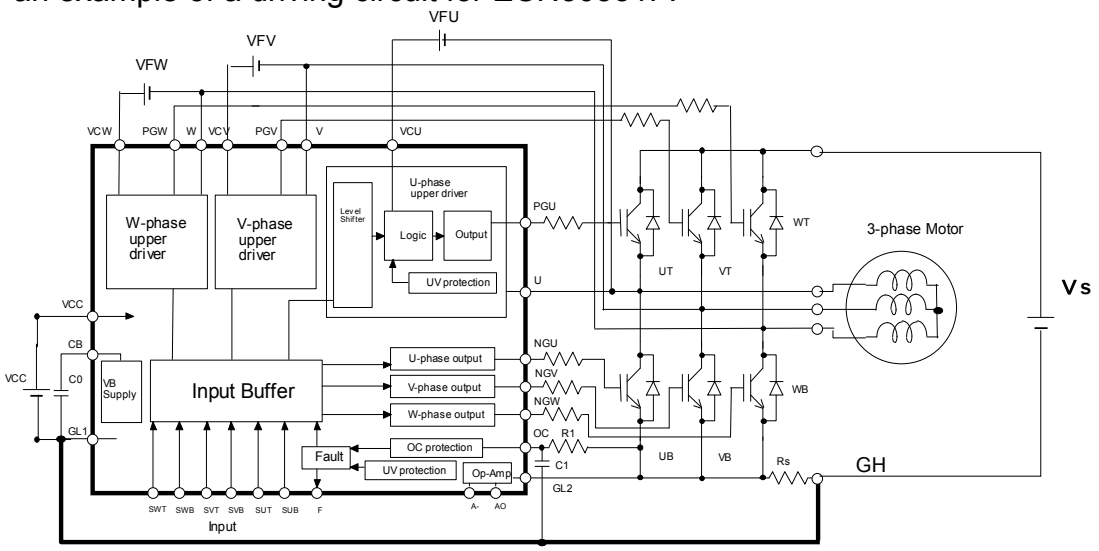

Figure 3.1.1 Example of a driving by a floating power supply (for ECN30531F)

3.2 Driving by a bootstrap system

Figure 3.2.1 shows an example of a driving circuit using a bootstrap system. External capacitors Cb are used for a power supply to operate top arm driving circuits. One side of Cb is connected to the source of IGBTs to allow the driver circuit to have higher voltage than Vs.

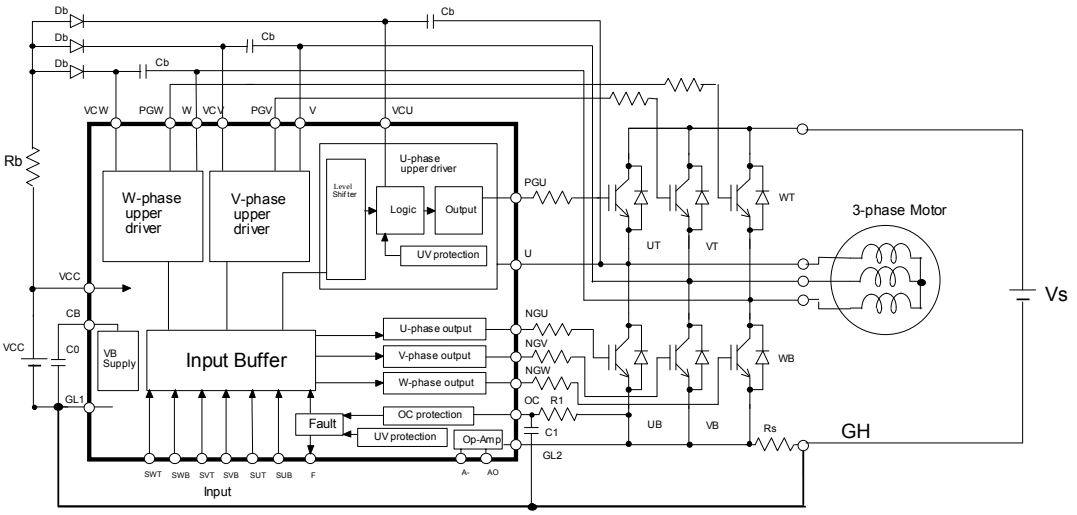

Figure 3.2.1 Example of a driving by a bootstrap system (for ECN30531F)

Cb is charged by Vcc. The cost of a bootstrap drive is lower than that of a floating drive, however, a bootstrap drive needs to charge the capacitors for driving top arms at the beginning of the operation. And the maximum time for turning on top arm devices is limited by the value of Cb.

4. Internal block and functions

Using the example of a bootstrap drive in Figure 3.2.1, internal functions are explained below.

4.1 Input buffer

An ECN30531F package has a total of six input terminals : three top arm device inputs(each marked with a T) and three bottom arm device inputs(each marked with a B). SUB, SVB, SWB are U, V, W phase inputs for the bottom arm devices, respectively. SUT, SVT, SWT are U, V, W phase inputs for the top arm devices, respectively. Correspondence of these input terminals with output ones are shown in Table 4.1.1. The six input terminals are pulled up by a resistance (typ. 200k-ohm) in the internal circuit. Table 4.1.2 shows the pulled up voltage. When

ECN30531F/30541F are connected to a microprocessor directly, a pull up resistance RH is needed for 6 inputs terminals as shown in Figure 4.1.1, in order to avoid a breakdown and a latch-up of output ports on a microprocessor. In Figure 4.1.2, when the output signal of a microprocessor is low, current flows through RH.

Table 4.1.1 Terminals and output terminals

Arm	U-phase	V-phase	W-phase
Top	SUT: PGU	SVT: PGV	SWT: PGW
Bottom	SUB: NGU	SVB: NGV	SWB: NGW

Table 4.1.2 Pulled up voltage for input terminals

Type	Pulled up voltage
ECN30531F/30541F	Vcc

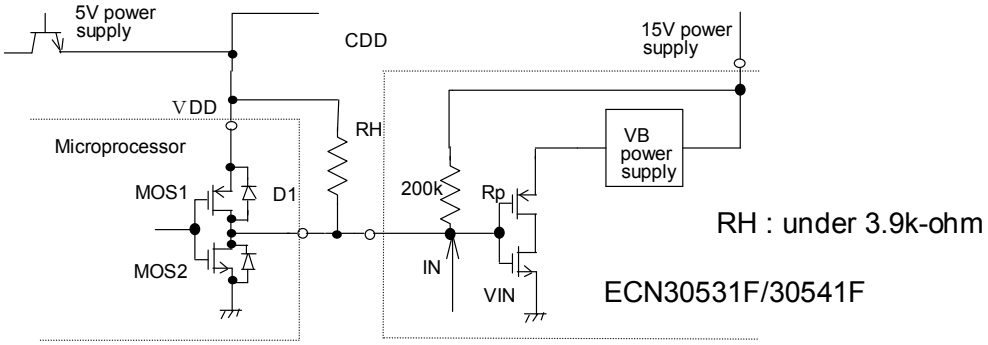

Figure 4.1.1 Example for pulling up at a direct connection to a microprocessor

In ECN30531F and ECN30541F, this current is becomes more than 1mA. In order to avoid this, a resistance for dividing voltage can be used as shown in Figure 4.1.2. For example, when R2 is 22k-ohm and R1 is 10k-ohm, Is becomes 0.68mA. The output signal of the IC is high when the input is low. Therefore, the external device is turned on when the input signal is low. The output device should be a device, like a n-channel IGBT, a n-channel MOSFET and so on, which can be turned on by a plus gate voltage against the source voltage.

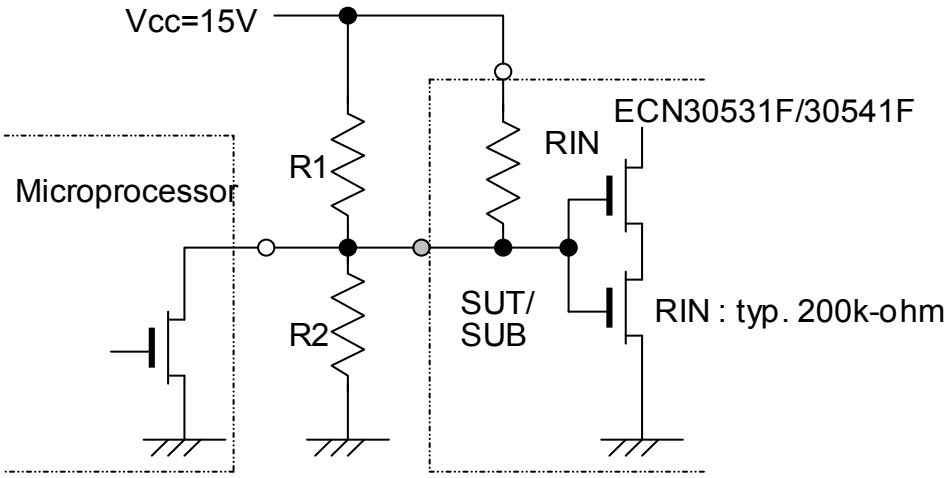

Figure 4.1.2 Configuration for R1 and R2

4.2 Dead time

As shown in Figure 3.1.1, the external devices at each phase are composed in such a way that the top and the bottom arm are built up like a totem pole. This makes it necessary to prevent the top and the bottom arm from turning on simultaneously at any instant when one arm(top or bottom) is switched on while the other arm(bottom or top) is on. In ECN30531F/30541F, on the other hand, a dead time is not generated internally. Therefore, a dead time must be set at the input signal side. The dead time must be at least double the sum of the ON/OFF delays of the internal and external output devices (except when such delays increase due to high temperature.)

4.3 Level shift circuit

The top arm control circuit is operated under floating voltage of “output voltage of the external device + control voltage Vcc”. The level shift circuit converts input signals based on the ground level into top arm drive signals based on output voltages of each phase that constitute floating potentials. Inside the IC, a latch circuit is equipped with an edge trigger for top arm input signals in order to reduce the power consumption of the level shift circuit.

4.4 Output section

The external output devices can be regarded as capacitive loads. Therefore, an IC output circuit needs source and sink operation. ECN30531F/30541F series incorporates a C-MOS type IC output. For both the top arm and the bottom arm, the value of the current ability is as follows,

Source current : 0.25A(typ.)

Sink current : 0.5A(typ.)

The amplitude of the bottom arm output voltage is nearly equal to Vcc, and the amplitude of the top arm output voltage is “the output voltage of the external devices (voltage at U, V, W terminal) + about Vcc”.

4.5 Protective function

4.5.1 Bottom arm under voltage protection

When Vcc falls below the under voltage detection level(10.5V typ.) for bottom arms, the protective circuit turns off the output voltage of all the arms and sets the fault output terminal logic to L. When Vcc exceeds the under voltage detection level plus hysteresis voltage, the fault output signal is set to H again.

4.5.2 Over current protective function

When the input voltage of OC terminal exceeds a specified value for bottom arms (0.49V typ.), the protective circuit turns off the output voltages of all the arms and sets the fault output terminal logic to L. Until the reset is operated, the fault output is latched to L. The over current protection current setting level (IOC) is determined by the following equation,

IOC=VOC/RS (A) (Rs is an external resistance.)

Inside OC terminal which is the input for VOC signal, a filter of 0.4μs is equipped. When over current protective function works by mistake due to some noise, an external filter with R1 and C1 should be added. Please see Figure 4.5.2.1 for its configuration. Please be careful that the time to detect over current sense signal is delayed, if R1 and C1 are too large.

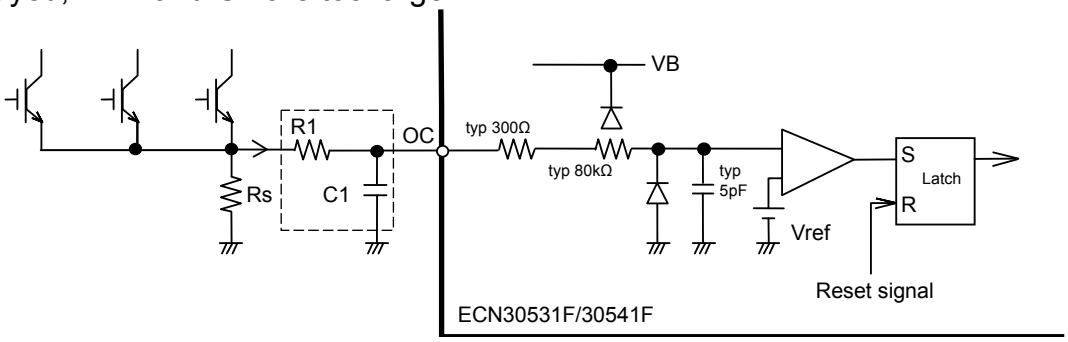

Figure 4.5.2.1 Configuration for R1 and C1

4.5.3 Top arm under voltage protective function

When any of the potentials VCU-U, VCV-V, and VCW-W falls below the under voltage level (10.5V typ.) for top arms, the protective circuit turns off the output voltage of the top arm of the corresponding phase only. In this case, the fault output remains unaffected.

4.5.4 Fault output terminal

This terminal is an open drain of n-MOS. Please pull it up via an external resistance Rf as follows. Rf should be more than 5.6k-ohm.

ECN30531F/30541F : to Vcc. CB or 5V

(Please refer to Figure 4.5.4.1.)

When an opto-coupler is connected to this terminal, it should be connected between CB and Fault as shown in Figure 4.5.4.2. The Fault output current should be 5mA (typ.) and a limiting resistance Rfc of 1k-ohm should be connected.

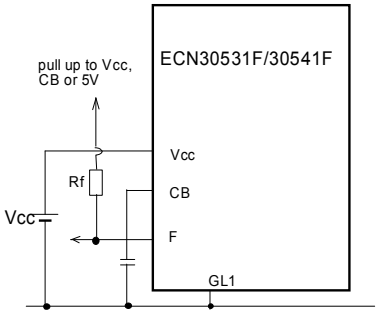

Figure 4.5.4.1 Configuration for a pull up resistance to Fault

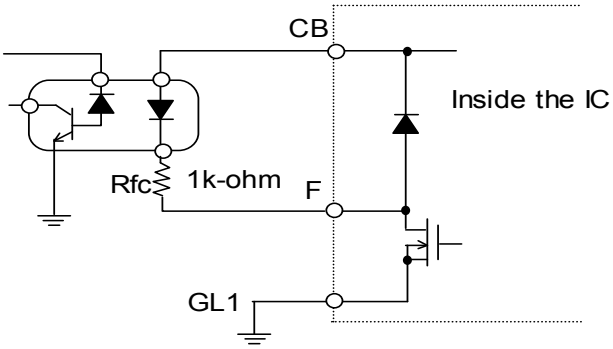

Figure 4.5.4.2 Configuration for an opto-coupler

To reset a fault output which has reached the L-level, please set all of the six input terminals of the top and the bottom arm to H. (This reset can also be triggered by turning on the Vcc again.) Table 4.5.4.1 shows the truth table for reset input, OC, under voltage protective operation for bottom arms and Fault output.

Table 4.5.4.1 Truth table for Fault output

Reset input	OC	Under voltage detection for bottom arms	Fault
0	0	0	H
0	0	1	L
0	1	0	L
0	1	1	L
1	0	0	H
1	0	1	L
1	1	0	L
1	1	1	L

In this table, Reset input “1” shows that 6 input signals for top and bottom arms are H-level. OC “1” shows that over current protective operation works. Under voltage detection for bottom arms “1” shows that under voltage protective operation for bottom arms works.

4.5.5 Operational amplifier (only ECN30531F)

ECN30531F incorporate an operational amplifier designed to amplify current sense voltage. Before using the operational amplifier, please add an external gain resistance in line with the internal circuit shown in Figure 4.5.5.1. If the operational amplifier need not be used, please connect A- to CB terminal in order to fix the output level of op-amp. In this case, the output of op-amp AO is 0V.

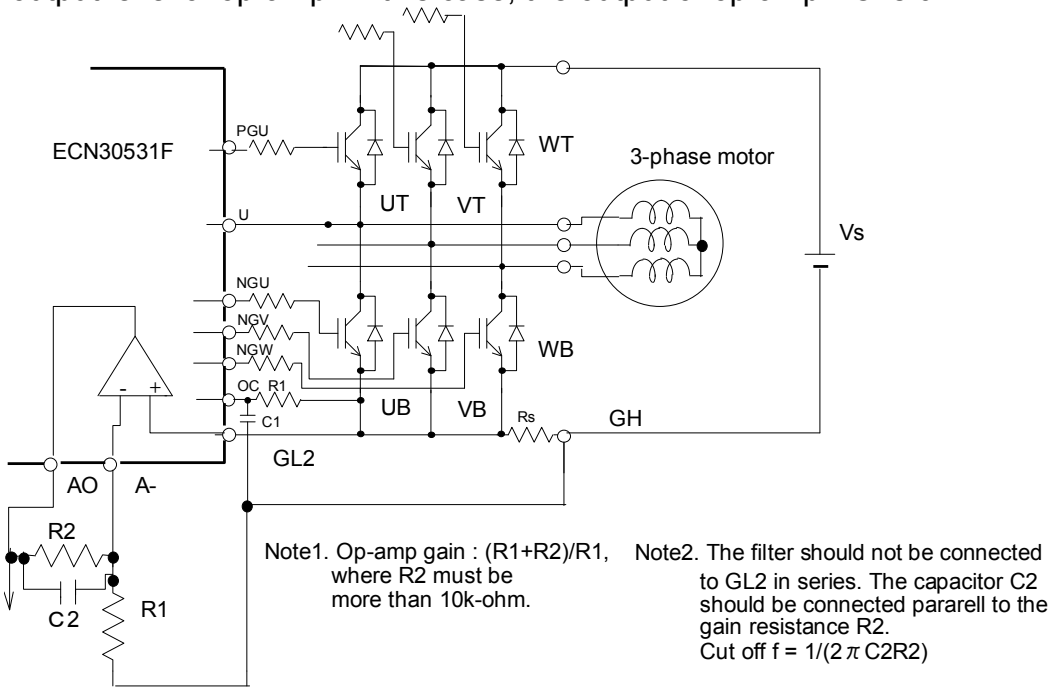

Figure 4.5.5.1 Configuration for using an Op-amp

4.5.6 VB power supply

The input buffer, bottom arm protective circuit, fault logic circuit and others are operated by an internal power supply voltage VB≅8V generated by the VB power supply circuit using Vcc. CB terminal must be connected with an oscillation-preventive capacitor Co (0.22μF or more).

4.5.7 Bootstrap circuit

The top arm drive circuit is powered by a bootstrap circuit. The charge pump and the bootstrap system are briefly explained below. The charge pump system charges capacitors C1 and C2 while the switches inside the IC synchronize with the frequency of the internal oscillator regardless of the action of the output device. In Figure 4.5.7.1 (a), SW1 and SW2 are high-voltage devices but there are no limitations to the duty of the output device. In the bootstrap system shown in Figure 4.5.7.1 (b), C3 is charged when the switching device externally mounted on the bottom arm is turned on. The ON duty of the output device is therefore generally limited, but the gate driver inside the IC requires no high-voltage device. Each chip of the ECN30531F/30541F series can use this bootstrap system. And as listed in Item 3, a floating supply drive is also available in ECN30531F/30541F series. In this operation the duty of the top arm output device is not limited.

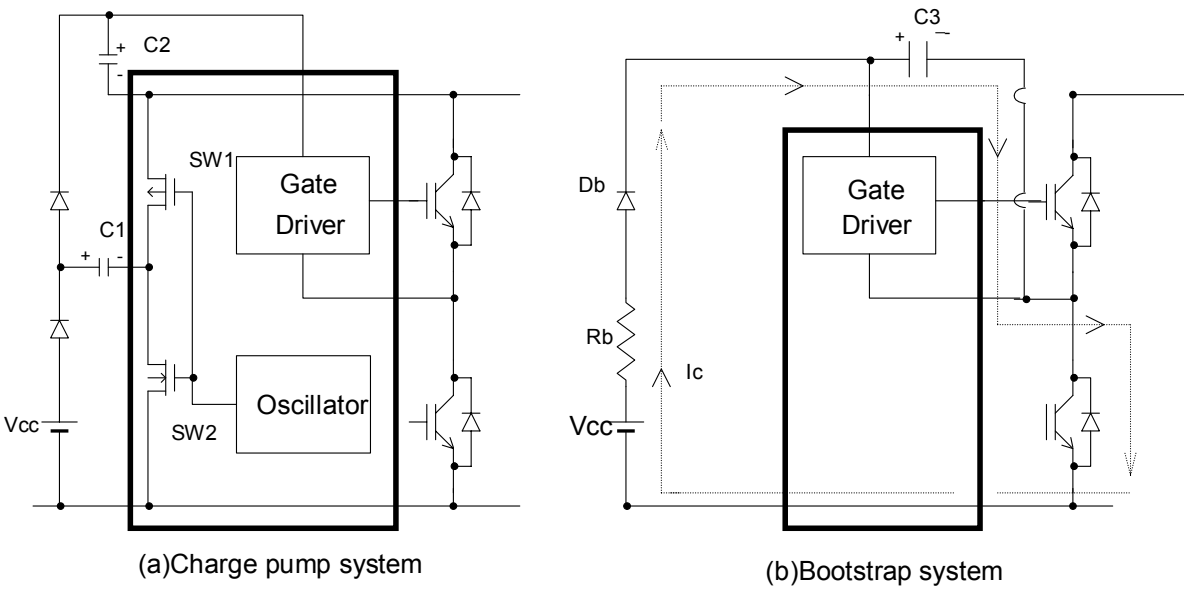

Figure 4.5.7.1 Power supplying to a top arm circuit

5. Power consumption and temperature rising

5.1 Power consumption

ECN30531F/30541F series has three types of power consumption as below,

- Power dissipation for charging and discharging the gate capacitance of the external IGBTs or MOSFETs which are loads for the IC.
- Power dissipation for operating level shift circuit, etc. in the IC
- Power dissipation for charging and discharging parasitic capacitance inside the IC

The rate of power dissipation for the external devices is under 10% of all power dissipation. When Vcc is 15V, Vs is 280V and input capacitance for the IGBTs is 1000pF, the change of power dissipation with PWM frequency is shown in Figure 5.2.1.

5.2 Temperature rising

From Figure 5.2.1, it can be seen that the power dissipation at a PWM frequency of 16 kHz is 0.17W. For SOP-28 packages, the thermal resistance on the glass epoxy print board R_{ja} is 84°C/W (print board size: 120×21×1.6mm, wire density 30%), therefore, temperature rise is 0.17×84=14.3°C.

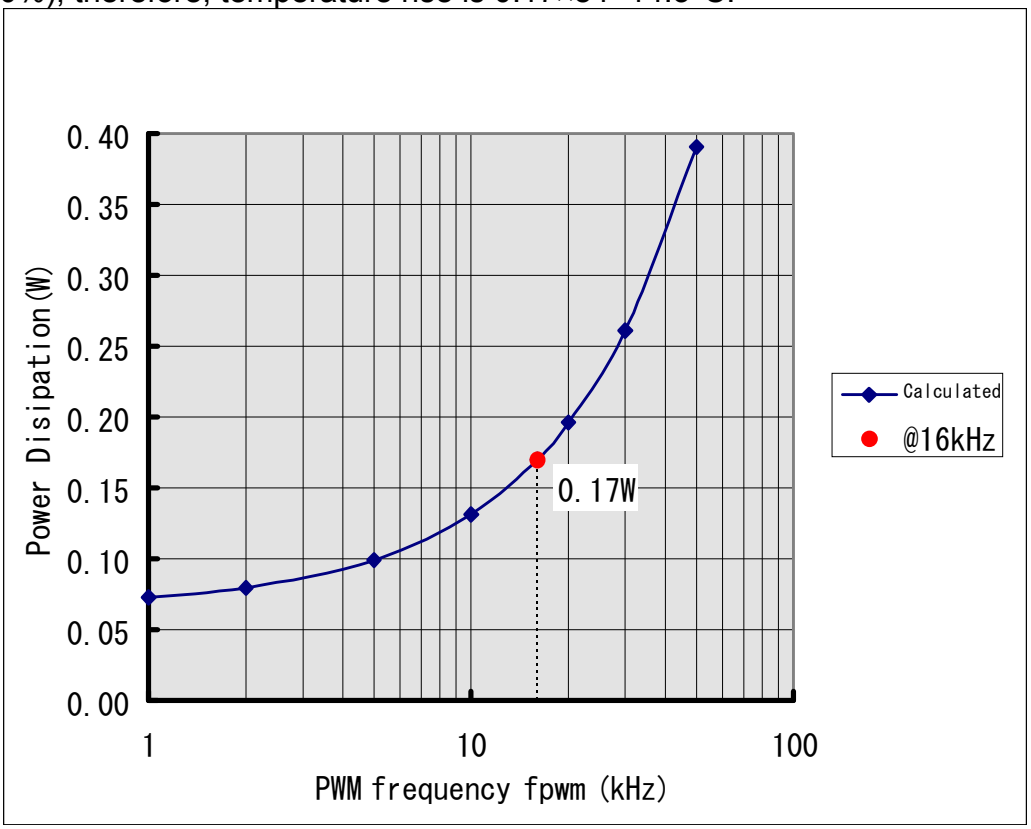

Figure 5.2.1 Power dissipation with PWM frequency

6. Precautions

6.1 Bootstrap capacitor : Cb, Current limiting resistance : Rb, Diode : Db

The capacitance of a bootstrap capacitor varies with switching frequency, the ON duty of an output device, and the gate capacitance of the external IGBTs or MOSFETs. A prolonged ON period of the top arm output device may lead to the top arm under voltage protective operation. For example, the longest ON time of the top arm output device is about 50ms when Cb is 3.3μF. Please refer to Table 6.1.1 for calculated examples. Cb should be connected to the IC as near as possible in order to prevent the IC from getting destroyed by excess voltage. Current limiting resistance Rb should be added because the maximum charging current in Cb should be under the allowed value of the surge current for Db and over current protective operation should not work at the beginning of the charging Cb. Resistance Rb(in Figure 4.5.7.1 (b)) should be more than a few ohms. Diode Db needs more than 600V breakdown voltage, very small forward voltage drop and short reverse recovery time Trr of under 100ns.

[Approximate value of Cb and maximum on-time for top arms determined by the value of IGBTs]

If the bootstrap charge voltage is operated at -1V of GL2 and the forward voltage drop of diode Db is 1V, Cb is charged to 15V when Vcc is 15V. Now it is named Q1 that is needed to fully charge the gate of IGBTs or MOSFETs to 15V. When the leak current of top arms is 30μA, the time that the voltage of Cb decreases from 15V to 12V, that is the maximum value of under voltage detection voltage for top arms, is the maximum on-time of top arms Tonmax. Therefore, the following equation can be determined,

$$15 \times Cb - Q1 - 30\mu A \times Tonmax = 12 \times Cb$$

The value of Cb should be chosen from the maximum on-time for top arms and all the electric gate charge to drive the gate of IGBTs or MOSFETs. Table 6.1.1 shows the calculated examples.

Table 6.1.1 Calculated examples of Q1 and Tonmax

Cb(μF)	Examples for output devices	Electric gate charge Q1(μC)	Maximum on-time for top arms Tonmax(ms)
1.0	500V/10A MOS	0.036	99
1.0	600V/30A IGBT	0.085	97
3.3	600V/30A IGBT	0.085	327
5.6	600V/30A IGBT	0.085	557

The Cb of 3.3μF having some margin is recommended. However, it should be determined after confirmation by evaluation.

Recommended devices ;

Db : 600V/1A, Trr=100ns

Cb : 3.3μF±20% [Stress voltage = 15V]

Rb : 3.3μF±20% [more than 2W]

6.2 Output wiring

The output wiring that connects the output terminal of the ECN30531F/30541F series to the external IGBTs or MOSFETs should be as short as possible in order to minimize the wire inductance. The frequency determined by the wiring inductance Lw and the gate capacitance Cg of the external devices oscillates the output wave form of the IC. When this oscillation voltage exceeds the maximum rating of the IC(for U-phase top arm output, for example, the PGU-U voltage is 20V, and for U-phase bottom arm output, NGU-GL1 voltage is 20V), the IC may get destroyed. Therefore, the following circuit elements should be connected near the top and the bottom arm output terminals of each phase of the IC as shown in Figure 6.2.1.

Capacitance CP = 560μF (If the wiring is about 30cm long, the value should be adjusted according to the wiring length. A ceramic capacitance should be used.)

Resistor Rg(in series with the gate) = 100 ohms (If an external IGBT of 20A or so is used, this value increases as the current rating of the external device decreases.)

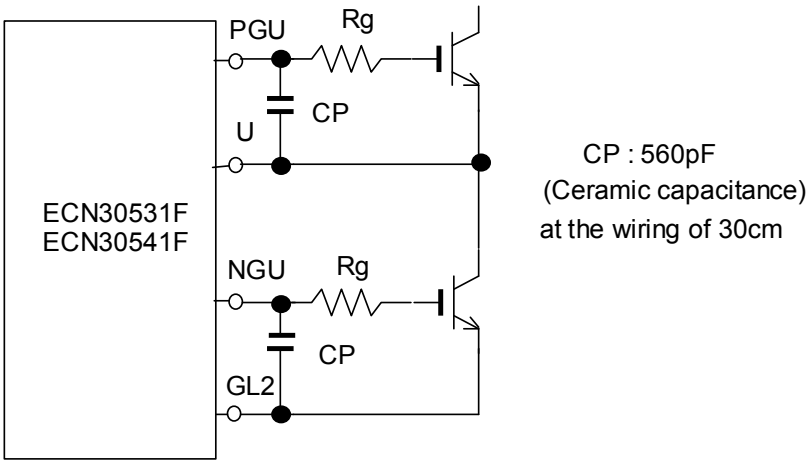

Figure 6.2.1 Adding an oscillation-preventive capacitance CP
(This figure shows the case of the U-phase alone)

6.3 Caution for noise at input terminals

6 input terminals tend to have an influence of switching noise from the external terminals because the input impedance is large. Therefore, when designing a print board, it should be careful that switching noise of external terminals should not affect the input terminals. When it is evaluated by a temporally wiring, the filters shown in Figure 6.3.1 should be connected to 6 input terminals. In this case, please confirm that the arm short circuit of the external devices does not occur because of the input pulse delay.

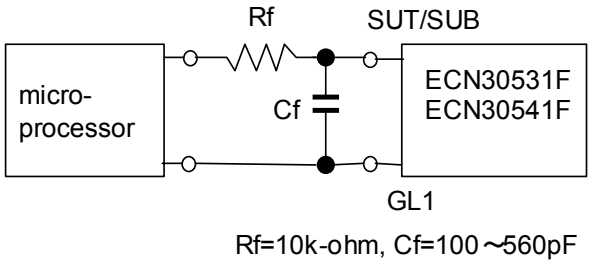

Figure 6.3.1 Adding filters for input terminals

6.4 Setting the bottom arm device input for bootstrap initial charge

Top arm drive circuits use the bootstrap system. Therefore, the top arm output device cannot be turned on unless the bootstrap capacitance Cb is charged to about 11V or more. When the power supply is turned on, the capacitance Cb is considered to be 0V in initial voltage. The Cb can be charged by turning on the bottom arm of the corresponding phase. The on-time of the reset for the bottom

arm can be determined from the impedance, Rb and Cb of the charging circuit marked with a broken line in Figure 4.5.7.1 (b). Generally, for the initial charge after turning on the power supply, the pulse width of three times as large as T=Rb×Cb for the bottom arm-on should be input, or more than 3 on-pulses of T=Rb×Cb for the bottom arm should be input.

6.5 Using external drive devices having a large capacitance

Connecting a C-MOS buffer to the IC output may allow IGBTs or MOSFETs of more than 30A to be driven. In this case, the quick switching of the output large-current device causes spike voltage or oscillation, which may result in the IC malfunctioning or the device is getting destroyed. When driving IGBTs or MOSFETs of more than 30A, please consult Hitachi about it.

6.6 Separating the high- and low-voltage ground wiring

In the block diagram and the external elements shown in Figure 3.1.1 and Figure 3.2.1, PWM voltage and current flows through the high-voltage ground wiring at controlling motors because Vs power supply deals with high-voltage and high-current. This high-voltage and high-current should not be flown through the ground wiring of Vcc which deals with low-voltage and low-current. Therefore, these ground wirings should be connected separately on the print board and should be provided with common line near the power supply. (Marked with the thick line connecting GL1 and GH at the bottom of Figure 3.1.1 and Figure 3.2.1)

6.7 Adding a capacitor for a power supply between Vcc and GL1

The noise voltage caused by L×di/dt of the wiring inductance may be produced at Vcc terminal of the IC and exceeds the maximum voltage, and may get destroyed. Therefore, a chemical capacitor should be connected near Vcc terminal of the IC. The value of this capacitance should be more than 10 times as large as the bootstrap capacitor Cb.

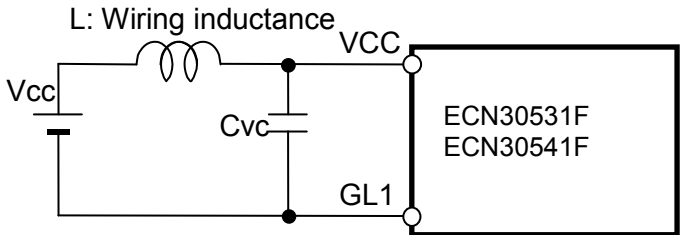

Figure 6.7.1 Adding a capacitor for power supply

6.8 Caution for no connection terminals

All the no connection(N.C.) terminals are not used for the connection inside the IC. However, they are parts of the parasitic capacitance for this IC due to the operation for this IC. Therefore, when wiring is connected to a N.C terminal on a print board, please consult Hitachi about it.

6.9 Insulation between pins

High voltages are applied between the pins of the numbers specified below. Apply coating or molding treatment.

ECN30531F: Pin No. 17-19, 21-22, 24-26

ECN30541F: Pin No. 16-18, 20-22, 24-26

Coating resin comes in various types. There are some unclear points as to how much thermal and mechanical stresses are exercised on semiconductor devices by size, thickness, and other factors of board shape, and the effects of other components. In selecting coating resin, please consult with your manufacturer.

6.10 Negative voltage at output terminal: NGU, NGV, NGW and GL2

Negative voltage between Rs and GND terminal could occur by inductive element of Rs shunt resistance or wiring. Especially, it may be tend to occur at phase changing timing of upper arm. In this case, regenerative current to power supply is main current.

In addition, this negative surge voltage may occur at PWM chopping of lower arm. This depends on the value of load current.

If this voltage exceed allowable rating of the IC, could lead to damage to the IC.

This is due to the negative voltage is applied between output terminal NGU, NGV, NGW of the IC and GL2 terminal.

Following method is recommended not to exceed 5V between NG* and GL1 terminal.

a) Please use no inductive type shunt resistor and make the wire length of the shunt resistor as short as possible.
b) Please put high speed type diode (trr<200ns) between Rs and GND terminal. Placing this diode between NG* and GL1 terminal of the IC is also effective. Current rating needs to be decided considering regenerative current.

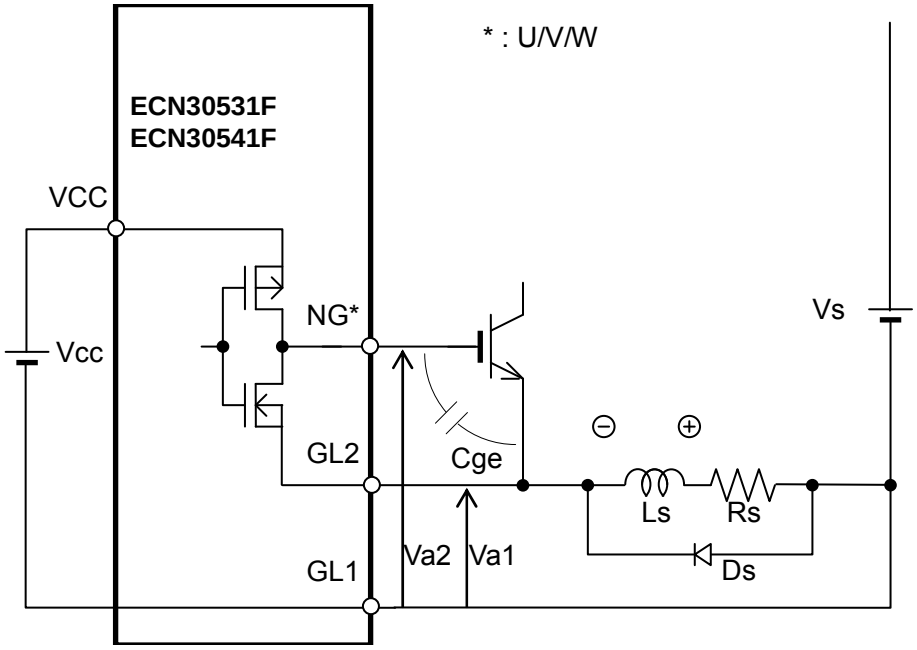

Figure 6.10.1 Negative voltage at output terminal (NGU, NGV, NGW and GL2)

6.11 Other precautions

Refer to "Precautions for Use of High-Voltage Monolithic ICs" for the other precautions and instructions on how to deal with products.

7. Notes Regarding This Document

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